JBL Professional Video Products

TECHNICAL TRAINING MANUAL MODEL 6810 AND 6820 VIDEO PROJECTOR

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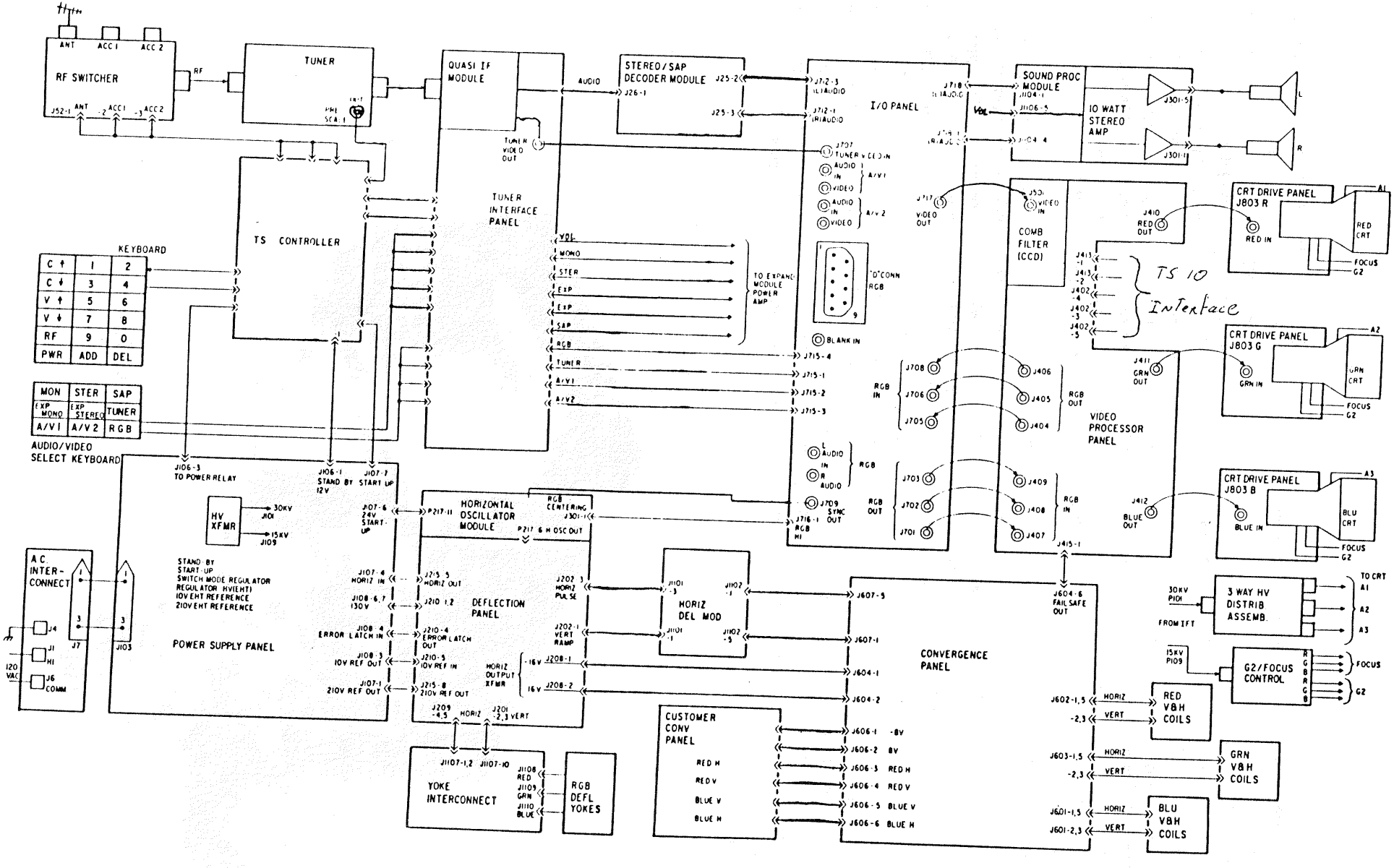


Figure 1 - Signal Flow Block Diagram

Signal Flow Block Diagram

The major functions of the projection TV system are shown in the Overall Block Diagram, **Figure 1.** The selected RF signal is fed from the RF Switcher to the Tuner and converted to Video IF. The IF Module, located on the Tuner Interface Panel detects both Composite Video and wideband Audio from the IF signal. The audio signal is fed to the Stereo/SAP Decoder Module, which checks for both Stereo Pilot and SAP FM carriers. To select either Stereo or SAP Audio, the appropriate button on the Audio Select Keyboard is pressed. Associated logic levels are sent from the Tuner Interface Panel to the Stereo/SAP Decoder and the Audio Processing Module to select the mode of operation. The selected Audio is decoded and fed to the I/O Panel Tuner Audio input J712-1, -3 where it is buffered, switched, and output at J718-1, -4. The Audio Processing Module, located on the Stereo Power Amplifier, processes the selected Audio. If the Stereo button was not pressed, the inputs to the Audio Processor remain in the Monaural mode. Audio Volume, Bass, and Balance controls adjust the drive to the Stereo Power Amplifier.

Detected Video from the IF Module is fed through the Tuner Interface Panel J32 to I/O Panel J707, the Tuner Video Input. The Composite Video signal is amplified, switched, buffered, and output at J717 for Video processing and J709 for Sync processing. The Composite Video is processed into Luminance, Vertical Detail, and Chroma signals. Luminance and Vertical Detail signals are matrixed and output at P501-5, -6, and Chroma is output at J501-10.

The Video Processor Panel receives positive Video, negative Video, and Chroma from the Comb Filter. These signals are processed into decoded R, G, and B Video, then buffered and fed from the Video Processor Panel outputs J406, J405, and J404 to I/O Panel inputs J708, J706, J705 respectively. Additional R, G, and B signal processing adds DC Restoration, Black Level, Sand Castle, and Vertical and Horizontal Blanking. The processed R, G, and B signals are buffered and fed to the individual CRTs through the CRT Drive Panels.

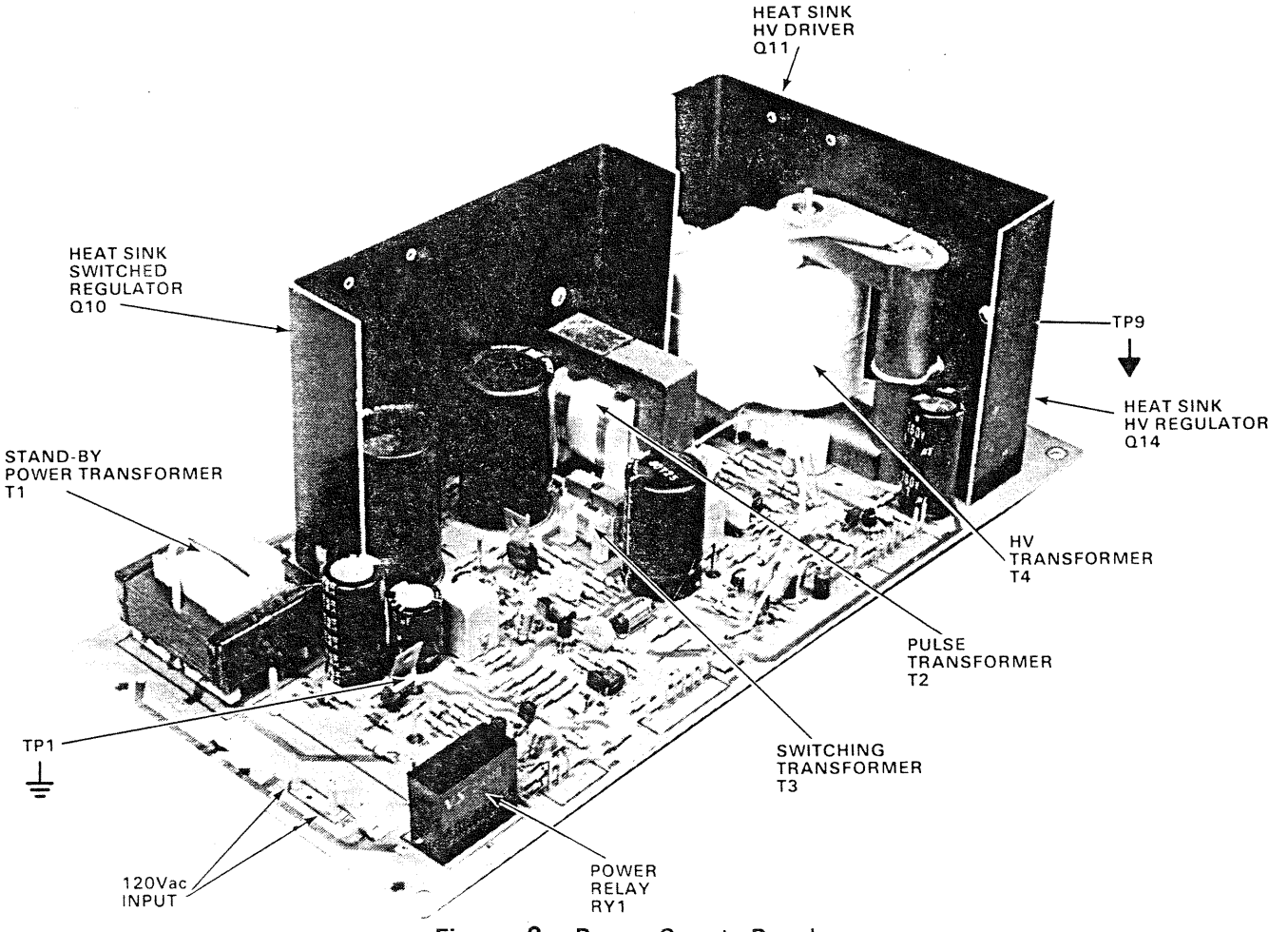


Figure 2 - Power Supply Panel

Power Supply Panel

The locations of major components on the Power Supply are shown in **Figure 2.** Starting in the lower left, they are: Stand-By and Start-Up Power Transformer; above is the heatsink, Switched Regulator, and Switching Choke; then the HV Transformer, HV Driver, HV Regulator and heatsink; on the right is the Panel pin-outs; below is the Power Relay.

The Block Diagram, **Figure 3**, shows the basic block functions of the Power Supply Panel. The Power Supply produces nine voltages (two of which are regulated), and one Error Latch circuit provides over-current and over-voltage shutdown. 120Vac is applied from the AC Interconnect board to the Relay Switch RY1, the 12Vdc Stand-By supply, and the 24Vdc Start-Up supply. The 12Vdc Stand-By Power is fed to the Tuner Controller and Tuner Interface Panel. The 24Vdc Start-Up voltage energizes the Deflection Panel and Tuner Controller. When the Power-On button is pressed, the Power Relay Control line activates the Power Relay, connecting 120Vac to the Voltage Doubler. The 310Vdc from the Voltage Doubler is fed to the Switched Regulator, which outputs the 130Vdc source voltage.

The Deflection Panel outputs Horizontal Drive pulses to the Optic-Coupler and drives the Switched Regulator. The Horizontal Drive pulses control the On time of the Regulator (and, therefore, the output voltage) by means of Pulse Width Modulation (PWM). The 130Vdc output from the Switched Regulator is fed to the Deflection Panel and High Voltage Regulator. The High Voltage Regulator controls the 30KV HV by regulating the 117Vdc input to the HV Transformer. The Horizontal Drive pulses are fed from the Switched Regulator to the Horizontal Drive circuit and the Horizontal Output transistor to develop flyback and scan pulses for the over-voltage shutdown and HV Regulator circuits. When an overload results from an overvoltage or overcurrent condition, the Switched Regulator is turned off by the signal on the shutdown line.

Initially, the Power Supply Panel provides 12Vdc Stand-By voltage to the Tuner Interface Panel and the Tuner Controller.

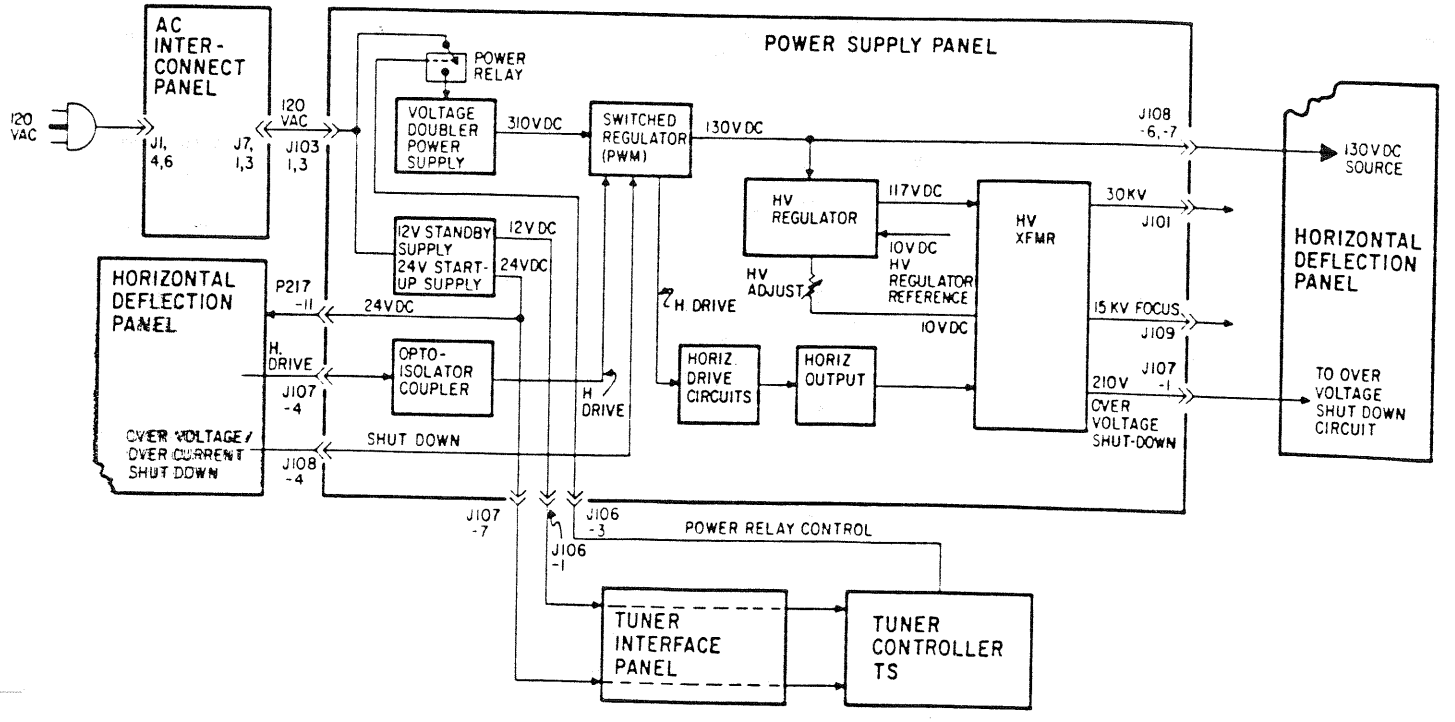


Figure 3 - Power Supply Basic Block Diagram

As seen in **Figure 4** the 12Vdc Stand-By voltage is applied to the 5V Regulator IC500-3 where it becomes the Keep Alive voltage for Microcomputer IC1000. The Relay control voltage and the 24Vdc Start-Up voltage are produced when the Power button is pressed. The key press is decoded by the Microcomputer IC1000 into a logic Low at pin 1, which turns Off Q19 and turns On Q20. The switching action of Q20 pulls the Power Relay RY1, Q3 and Q2 to ground. Q1 conducts and applies 24Vdc to the Power Relay. The relay latches and connects 120Vac to the Voltage Doubler. Q1 also supplies 24Vdc to the Horizontal Oscillator Module and Optic Coupler IC1 on the Power Supply Panel.

A pulse train, developed by the Horizontal Oscillator Module, drives the Horizontal sweep circuits and the Switched Regulator on the Power Supply Panel. R5 and C10 form a two second timing circuit. C10 begins to charge toward 42Vdc after the Power button is pressed. If the voltage on C10 reaches 15.8 volts before the scan derived voltages are developed, zener Z1 turns On. This places Q3 into saturation, removes Q2 forward bias and shuts down the Start-Up Supply. During this time period, if Horizontal Output Transformer T2 and HV Transformer T4 are driven, the flyback pulses are rectified and produce the derived voltages. A scan-derived 24Vdc from the Deflection Panel is fed through diode D6 to zener Z1 and turns Off Q1 while in the Run Mode. After the Stand-By and Start-Up modes are completed, the Run Mode takes over.

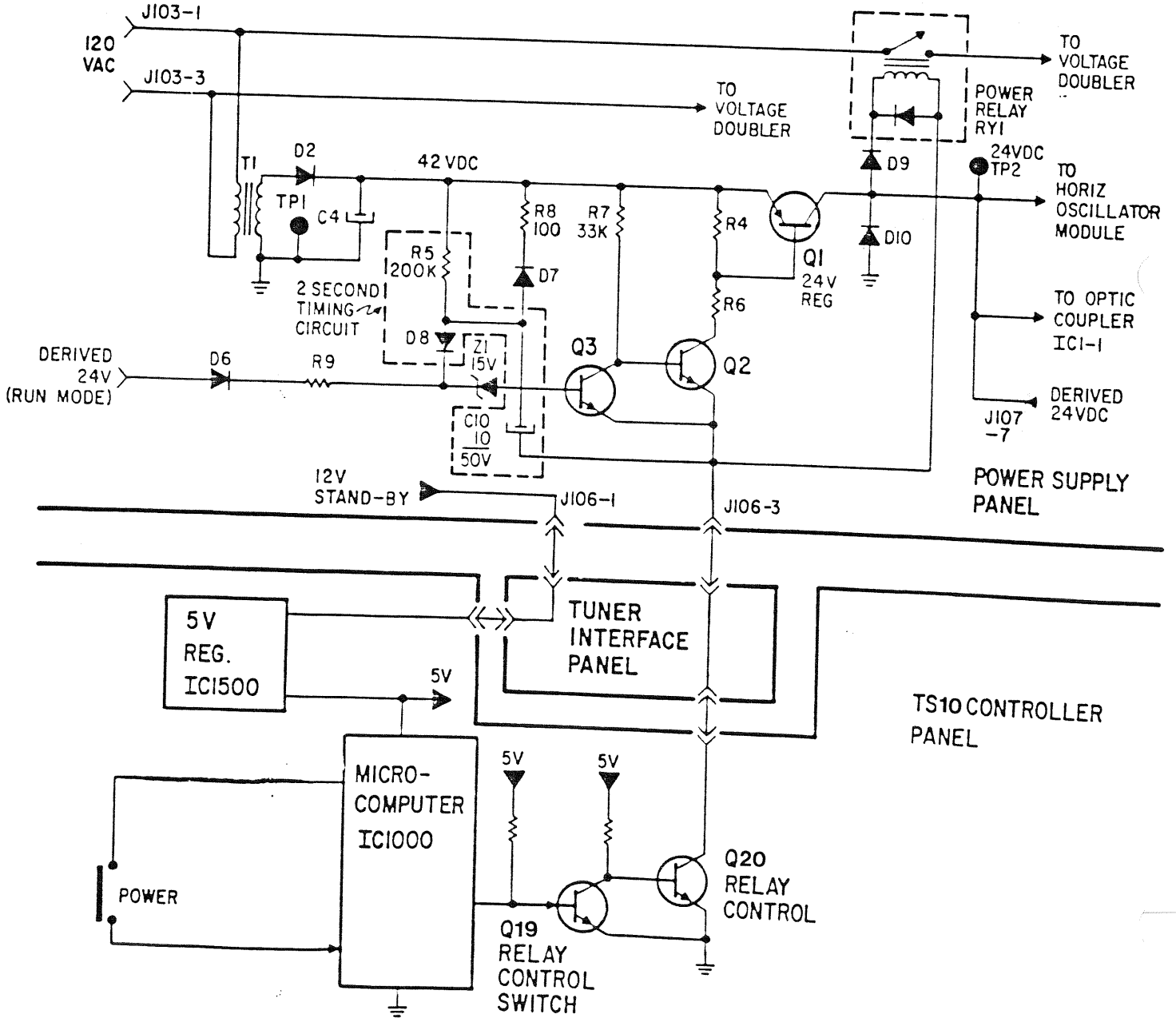


Figure 4 - Power On Circuit

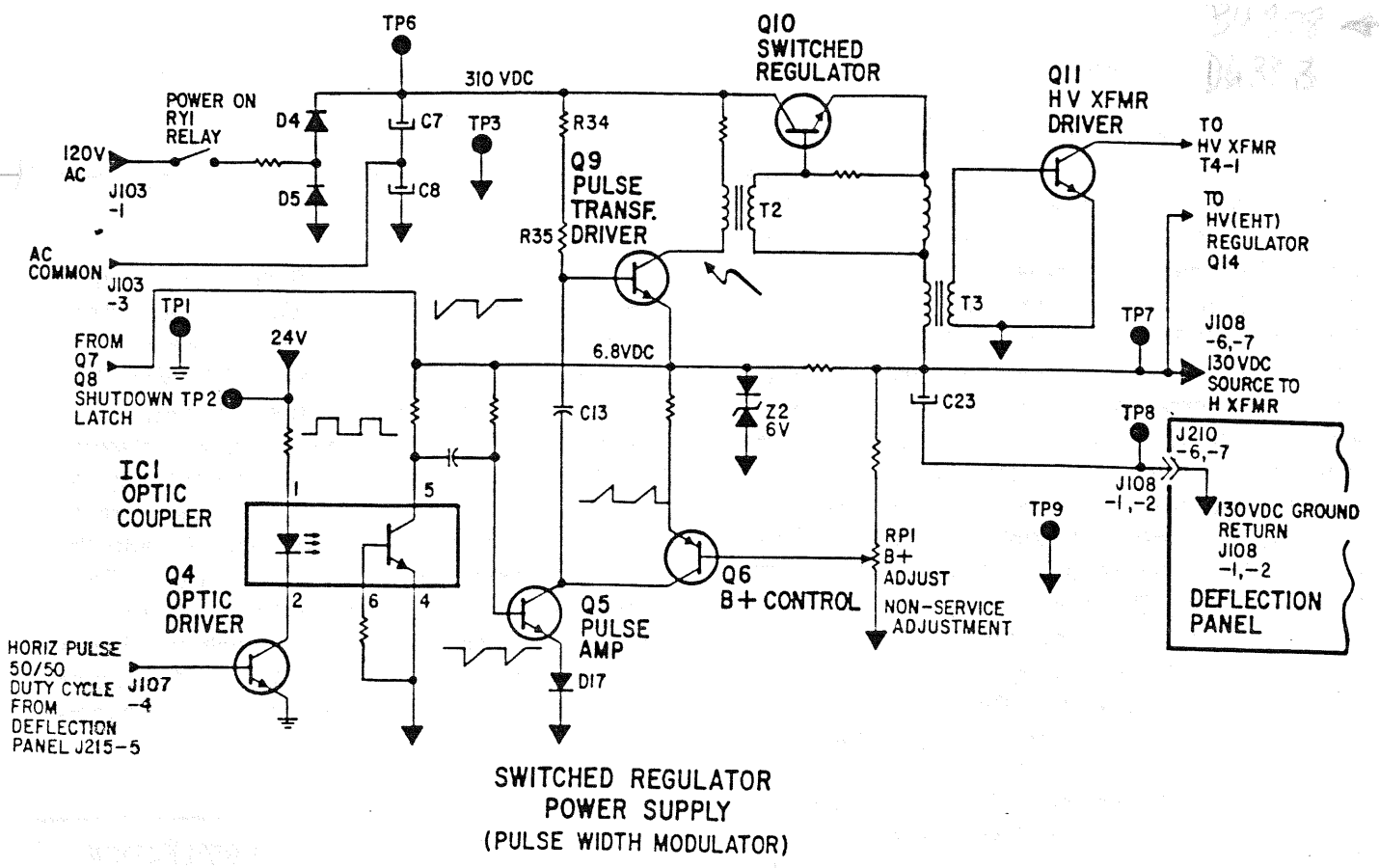


Figure 5 - Switched Regulator Circuit

Switched Regulator

In the Run Mode, drive pulses developed on the Horizontal Oscillator Module are fed to the Optic-Coupler Driver Q4, **Figure 5**. The 50/50 duty cycle pulse train is fed from the Deflection Panel through J215-5 and Power Panel J107-4 to Q4. Two ground systems are used in the Switched Regulator circuit to separate "ac" ground from "signal" ground. The Optic-Coupler, IC1, separates the circuits using different grounds by coupling signals from one circuit to the other with an LED/Phototransistor IC package. The major components in the Switched Regulator circuit are: the Optic-Coupler Driver Q4, Optic-Coupler IC1, Pulse Amp Q5, Ramp Capacitor C13, B+ Adjust RP1, B+ Control Q6, Pulse Transformer Driver Q9, Pulse Transformer T2, and Switching Regulator Q10.

The 310Vdc output voltage from the Voltage Doubler is used to charge the Ramp Capacitor C13, to forward bias Q9 through R34 and R35, and to provide collector voltage to the 130V Switching Regulator Q10. The regulated voltage at Q10 emitter and Test Point TP7 is adjusted to 130Vdc with RP1 B+ Adjust. The 130Vdc appears across an RC network that includes RP1, and is zenered to 6.8Vdc by Z2 for IC1 B+, Q5 forward bias, and Q9 and Q6 emitter voltages.

Q5 is switched On and Off by IC1 50/50 duty cycle pulse train. When Q5 is On, C13 is discharged and is clamped to the D17 voltage drop of 0.7Vdc. Q9 base is pulled negative, turning Off Q9. C13 begins to charge through R34 and R35. At Q5 turn-Off time, C13 discharges via Q6, holding Q9 On until Q5 is switched On to charge C13. When the charge and discharge of C13 remains constant, the switching pulse to Q10 base remains constant and the 130Vdc remains constant. However, if the 130Vdc increases, the voltage at RP1 wiper increases, turning down Q6. C13 discharge is less, and Q9 base is pulled less negative causing Q9 to turn On sooner. Q10 remains Off longer and the increased 130Vdc returns to normal. When the 130Vdc supply decreases, RP1 wiper feeds a lower voltage to Q6, turning it On harder, which permits C13 to discharge more. Q9 base is pulled more negative causing Q9 to turn On later. Q10 then remains On longer, raising the decreased 130Vdc to normal. the regulated 130Vdc is fed to the Horizontal Output Transformer T2-15 and HV Regulator Q14.

High Voltage Regulator

The HV Regulator circuit, **Figure 6**, is driven by a control circuit consisting of a voltage comparator Op-Amp IC2, HV (EHT) Adjust RP2, Differential Amp Q12, Q13, and HV Regulator Q14. "EHT" means Extra High Tension. The term is a reminder to the technician that the 30KV Projection CRT Anode voltage has high current capabilities, unlike conventional picture tubes, and that extreme caution must be exercised when working around HV Circuits. The voltage on the inverting (-) input of Comparator IC2 is adjusted by RP2 and compared to the non-inverting (+) input potential zenered to 6.8Vdc by Z4. The output voltage at IC2-6 is set by RP2 to balance the Differential Amp inverter stage Q13 to the non-inverting stage Q12, which is forward biased by 6.8Vdc from Z4 and D19. Q12 forward biases Q14 HV Regulator to output 117Vdc to HV Transformer T4-13. Regulation occurs when the 10Vdc (ETH) Reference voltage decreases or increases. If the scan-derived 10Vdc decreases, the decreased voltage at RP2 wiper and IC2-2 causes the Comparator IC2-6 output to rise and turn Q13 On harder, raising Q13 and Q12 emitter voltages. Q12 conducts less and its collector voltage rises, turning On Q14 to restore the 10Vdc (EHT) Reference by increasing the 117Vdc to HV Transformer T4-13.

When the 10Vdc (EHT) Reference voltage increases, the Comparator IC2-2 voltage rises and causes the IC2-6 output to decrease. Q13 conducts less and lowers both Q13 and Q12 emitter voltages, which then lowers Q12 collector voltage. Q14 conducts less and restores the 10Vdc (EHT) Reference by decreasing the 117Vdc to the HV Transformer. A large increase in beam current tends to lower the HV and the scan pulse amplitude used for the 10Vdc (EHT) Reference, and low beam current causes an increase in HV and the scan pulse voltage. These conditions are monitored by IC2, which initiates the correction for both conditions and maintains a constant 30KV HV to the CRTs.

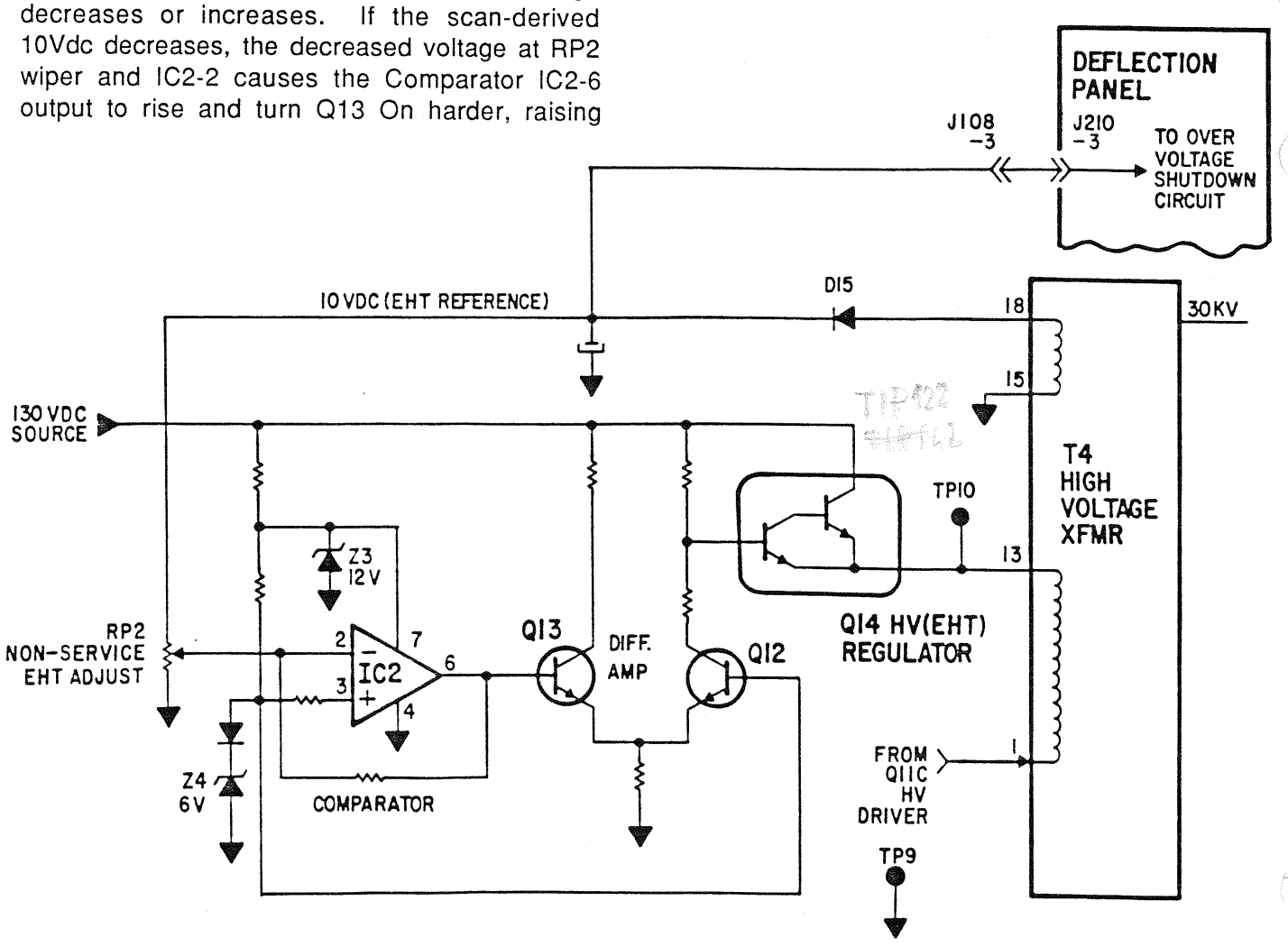


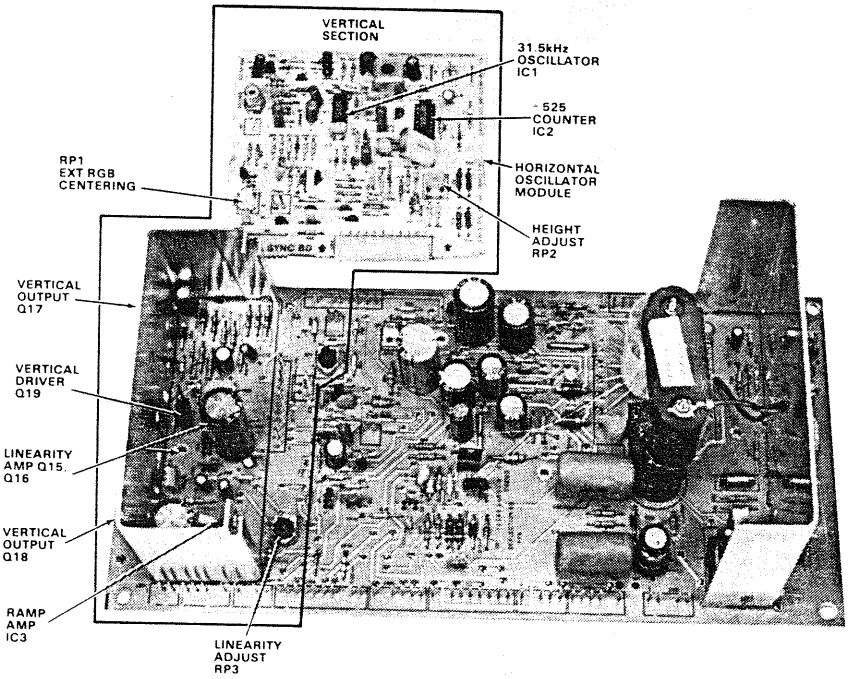
Figure 6 - High Voltage (EHT) Regulator Circuit

Deflection Panel

The photograph showing the Deflection Panel, **Figure 7**, calls out the power supply section and components. The panel is divided into Vertical sweep circuitry and the power supplies for the scan-derived dc voltages. The Horizontal Oscillator Module is attached and supported by the Vertical Output heaksink. Other major components are: the Horizontal Output Transformer T2, Horizontal Output Transistor Q10, Drive Transformer T1, Linearity Coil L2, Pre-Driver Q8, Driver Q9, and Scan Pulse Rectifiers D15 through D20.

Horizontal Oscillator Module

The circuits of the Horizontal Oscillator Module are shown in **Figure 8**. The internal function of IC1 are: Sync Separator, Video Amp, AGC, Noise Inverter, Phase Shaper, Phase Control, and the 31.5KHz Oscillator. the 31.5KHz Oscillator frequency is adjusted with coil L1, while the Oscillator Set-Up test point TP2 is jumpered to ground. Grounding TP2 allows the oscillator to free-run and causes the picture to roll vertically. L1 should be adjusted until vertical roll stops, or nearly so. When the jumper is removed from TP2, the picture will lock.



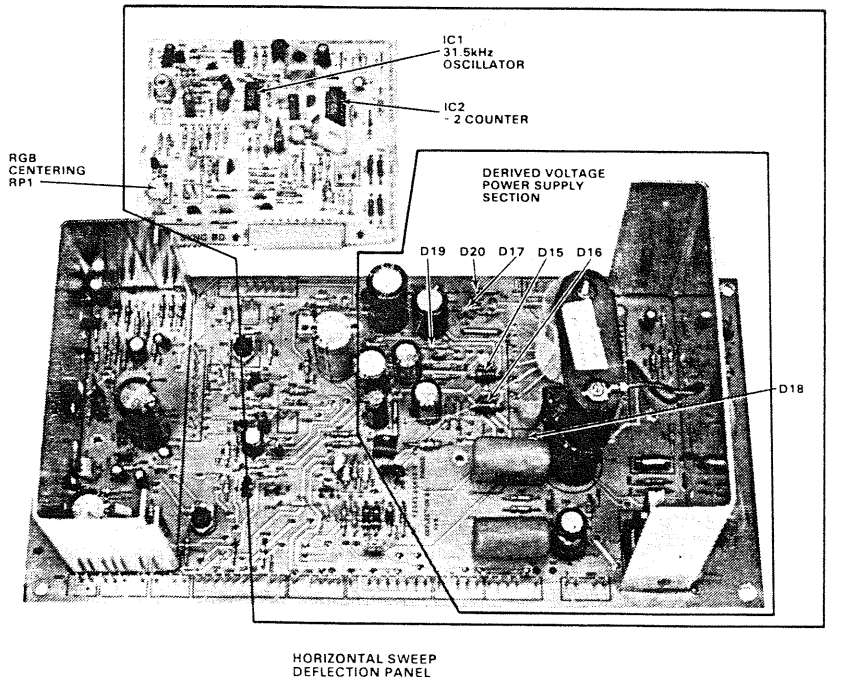


Figure 7 - Deflection Panel

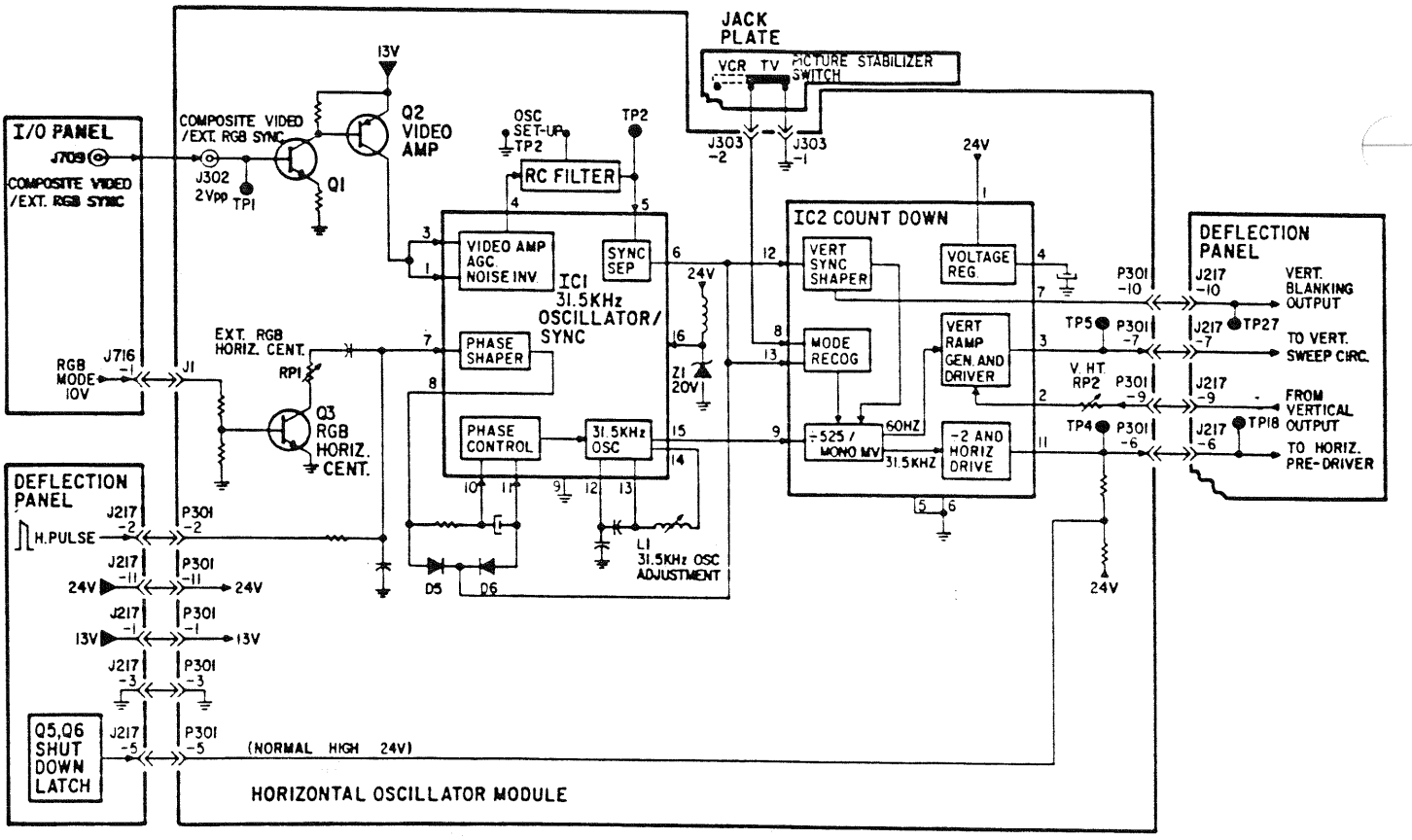


Figure 8 - Horizontal Oscillator Module

The Sync signal from the I/O Panel J709 is input at J302 and can be either Composite Video or Composite Sync, depending upon the program source. Either signal is 2Vpp ac-coupled to Q1. Q2 collector outputs 4Vpp negative Composite Video to IC1-3 and -1. The signal is inverted, amplified, buffered, and coupled to Pin 4 at 5.5Vpp. The external network at Pin 4 limits the high and low frequency information going into IC1-5. Sync is removed by the Sync Separator, buffered and fed to IC1-6. Internal AGC keeps the Sync tips as a constant level.

The 31.5KHz Oscillator signal is coupled to the Count Down IC2-9 and Composite Sync is fed to the IC2-12 and -13. If the Sync signal is standard NTSC Sync, the Mode Recognition circuit selects the Divide-by-525 Mode. The 31.5KHz signal at IC2-9 is counted down to 60Hz, which triggers the Vertical Ramp Generator and develops drive for the Vertical Sweep circuit. The 31.5KHz pulses are also applied to a Divide-by-2 Counter to produce the Horizontal Drive signal. If the Sync pulses fed to IC2-13 are not standard NTSC Sync, the Mode Recognition switches from the Divide-by 525 Mode to the Integrated Signal Mode. The integrated signal at IC2-12 triggers a Monostable Multivibrator which, in turn, locks the Vertical Ramp Generator to the non-standard Vertical Sync signal.

Picture jitter can result from poor NTSC Sync, non-standard Sync, or noise. To stop the jittering, a Sync Stabilizer switch on the control panel can be placed in the On position which pulls IC2-8 from ground and switches the Mode Recognition circuit to the Integrated Sync Mode.

Vertical Sweep Circuit

The Vertical Sweep circuit is shown in **Figure 9** and consists of a differential Amplifier Q15 and Q16, Vertical Driver Q19, and Complementary Push-Pull Output Transistors Q17 and Q18. Q15 and Q16 form a differential input. A 2Vpp vertical rate sawtooth from P310/J217-7 drives Q15; its collector signal drives Q19, which drives Q17 and the Vertical Yoke windings. Yoke current flows through the series resistor R117. The voltage drop across R117 is applied to the Vertical Linearity circuit. Vertical Linearity is adjusted by RP3. RP3 and C81 reshape the feedback signal to correct raster linearity at the top half of the picture.

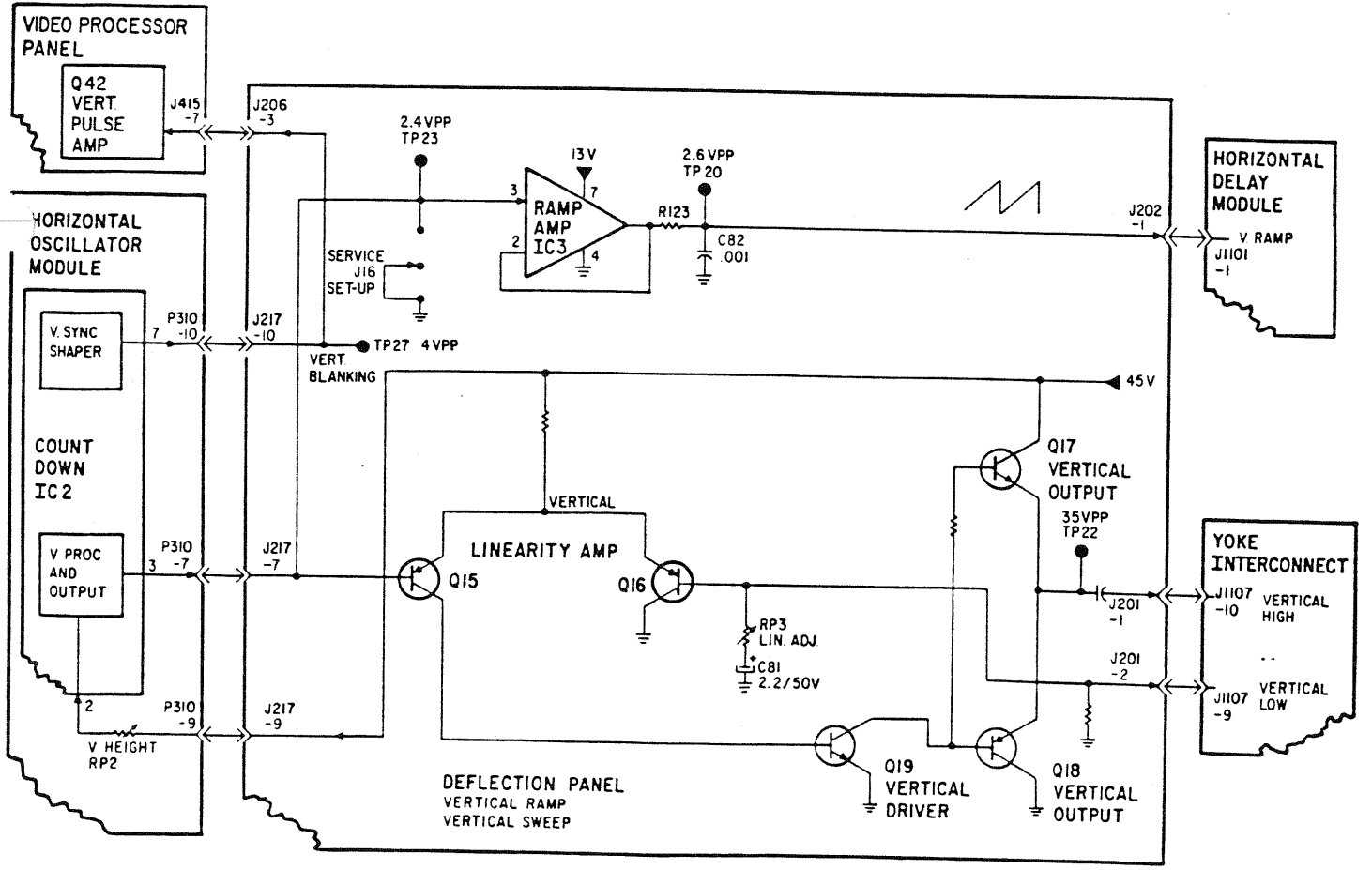


Figure 9 - Vertical Sweep Circuit

Horizontal Sweep Circuits

Both Vertical and Horizontal Drive signals are coupled from the Horizontal Oscillator Module to the Deflection Panel through J301, as seen in **Figure 10**. Horizontal drive from P301/ J217-6 is fed to Pre-Drive Q8. Collector voltage for Q8 and Q9 comes from the 24Vdc Start-Up supply. The signal at the collector of Q8 is ac-coupled by C39, clamped by D12, and applied to the base of Q9. Transformer T1 serves to isolate the Hot Ground circuits from the Cold Ground circuits. The step-down transformer, T1, provides about 6.5Vpp drive to the Horizontal Output Transistor, Q10. Sweep voltage is coupled through the Yoke Interconnect board to the Horizontal windings of the Deflection coil.

Six dc voltage sources are derived from the Horizontal Output Transformer. Scan pulse rectifier diodes D15 and D16 develop 16Vdc and -16Vdc respectively. D17 develops 24Vdc, D18 develops 13Vdc, D19 develops 200Vdc, D20 develops 45Vdc and 40Vdc is derived from the 45Vdc source.

Overload Protection Circuits

The Overload Protection circuits shown in **Figure 11** switch Off the 130Vdc supply when excessive current is sensed in the 130Vdc supply L2 on the Deflection Panel.

During normal operation, the 10Vdc (EHT) Reference voltage is fed from Power Panel J108-3 to D10, charging C37 and C38 to about 7VDC. Simultaneously, the Horizontal Yoke current flowing in the Horizontal Linearity coil develops a 9Vpp pulse, which is limited by Z8 should it exceed 20Vpp. The Yoke pulse is rectified by D9 and charges C36 to about 7Vdc. Q7 is turned On and pulls the junction of R52 and R55 to ground, which holds the Error Latch Q7/ Q8 Off.

Should a Horizontal sweep failure occur, capacitor C36 discharges. When its voltage reaches about 5Vdc, the Error Latch Driver is turned Off and the junction of R52/R55 is removed from ground. Q8 is turned On and shorts the 6.8Vdc source, which cuts Off the Switched Regulator Q10 and the 130Vdc supply.

In a similar manner, when the Protection Circuit detects an excessive current flowing in the 130Vdc supply, the Error Latch is turned On. or when there is a loss of Horizontal scan. The Error Latch circuit components are: the Error Latch Q7/Q8, Over-Current Sense R30/ D23/ D24, Latch Driver Q7, 10Vdc (EHT) Reference capacitors C37/C38, and the Yoke current pulse voltage developed by the Horizontal Linearity coil

The Switched Regulator and the scan-derived voltages from the Horizontal Output Transformer are killed; only the Stand-By 12Vdc supply remains active. the 24Vdc Start-Up supply is On, but it is inactive until the Power Button is pressed. To reset the circuit, the power cord is removed from the 120Vac power socket, reinserted and the Power button is pressed.

TS-10P Tuning System

The TS-10P Tuning System, **Figure 12**, is designed exclusively for Projection TV. The major components of this system are the 178-channel Controller, the Tuner, and the Tuner Interface Panel. The Controller uses an 8-but Microcomputer, a CITAC IC, a Microprocessor with internal ROM for processing On-Screen data, and a Graphics Generator/Matrix IC to receive the On-Screen data and create the On-Screen graphics Video signal.

The IR Remote Transmitter has 40 pushbuttons as seen in **Figure 13**. The system performs 35 functions with the On-Set Keyboard and 64 functions with the 40-pushbutton Remote Transmitter. The functions controlled by the 40 button Transmitter are: Power On/Off, Random

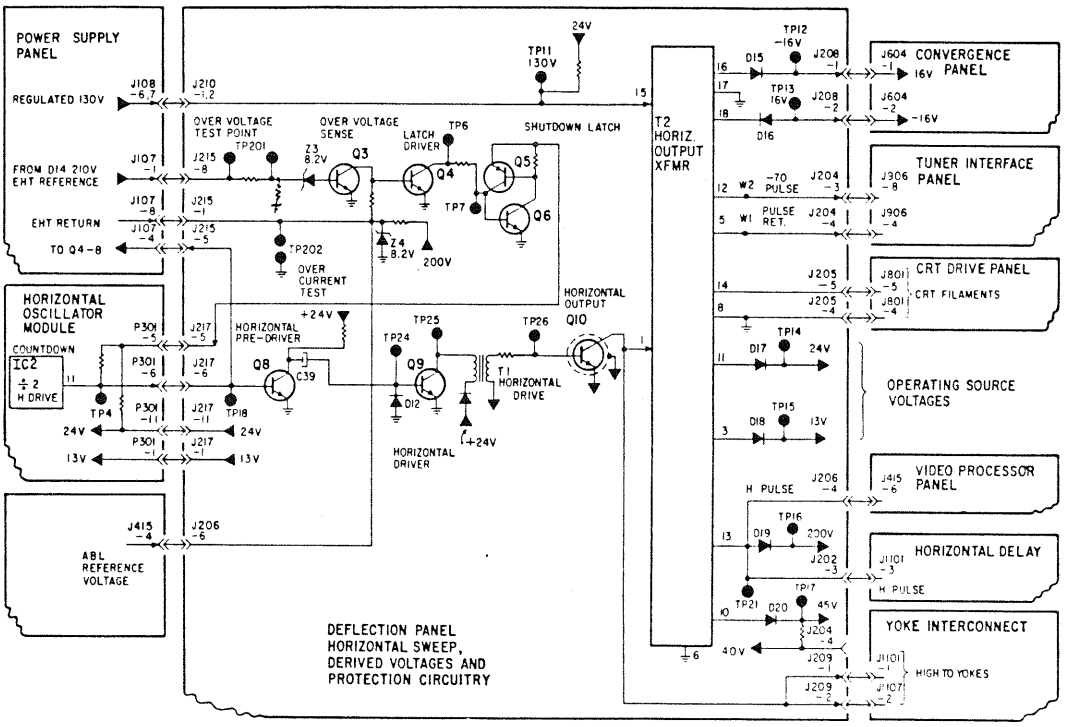


Figure 10 - Horizontal Sweep Circuit

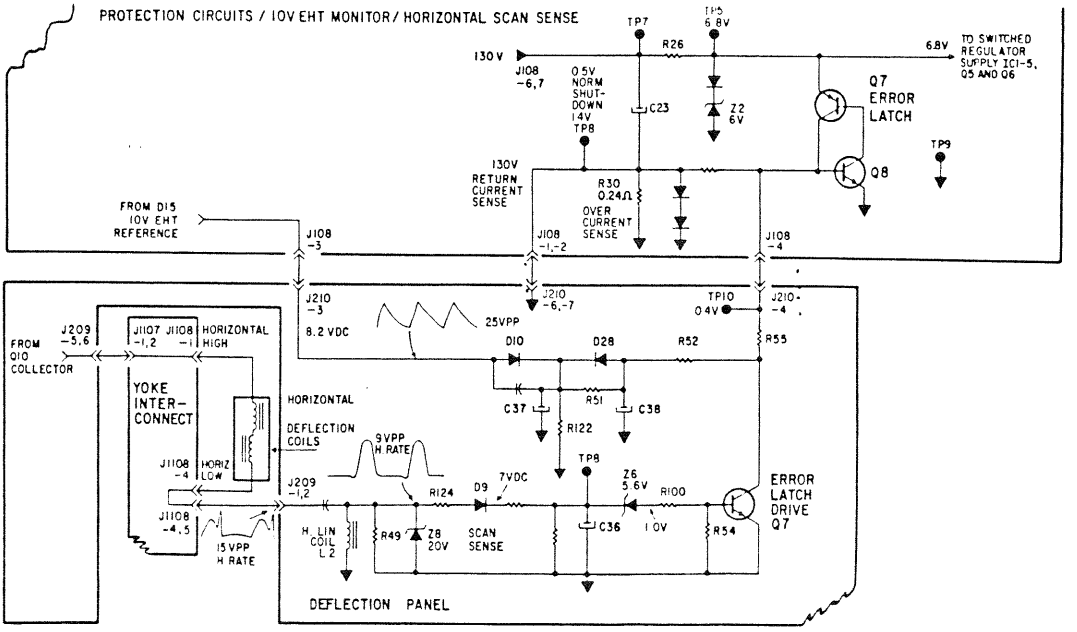


Figure 11 - Overload Protection Circuits

Channel selection, Channel Scan Up/Down, Mute, Alternate Channel (Quickview or Review), Recall, Balance, Bass, Treble, SAP selection, Mono/Stereo selection, Expanded Sound selection, Antenna/Accessory 1/Accessory 2, RGB, A/V1/ A/V2, Personal Preference, Volume Up/Down, Brightness, Picture, Color, Tint, and 100 (for selecting channel numbers 100 and higher). The TS-10P Tuning System will tune 56 UHF channels in the Broadcast mode and 122 channels in the Cable mode, which includes the twelve VHF broadcast channels.

The Channel Scan buttons place the Micro- computer into a two-speed scan mode. the first five channels are scanned at two channels per second. thereafter, the channels are scanned at ten channels per second until the button is released. Sound is muted when a Scan button is depressed. Unmuting is accomplished when the button is released.

The On-Screen channel numbers appear in the upper left corner of the Viewing Screen in yellow with the leading zeros suppressed. Clock infor- mation is displayed in the lower right corner, also in yellow. Four dashes indicate either a power failure or an invalid time entered into the clock. The time with colons flashing indicate the clock is running. Broadcast/Cable information appears below the channel number. "Normal," in red, indicated the Broadcast mode, while "Cable," in green, indicates the Cable model. the valid Channel Entered display will be presented for two seconds. Subsequently, the Broadcast/Cable and Clock information will disappear, while the channel number will shrink to the left and extinguish.

When the Power On button is pressed on the Transmitter or the Keyboard, a coded signal is sent to the Microcomputer. The signal is decoded into a logic Low at IC1000, **Figure 14**, which energizes the Power On relay and connects 120Vac to the TV power supply. When the Horizontal sweep system and/or the chassis power supplies come On, signals and voltages are fed to the Controller via the Tuner Interface Panel.

The 10Vdc Stand-By Voltage from the TV Power Supply Panel keeps the Microcomputer alive during the power Off periods and maintains the Last Channel Viewed and Volume Level memories. The chassis is powered On by a microcomputer-controlled relay. The CITAC IC controls bandswitching, channel tuning, volume, muting, bass, treble, and balance; it also controls brightness, picture, color, tint, and the RF Switcher. Volume is controlled in 64 steps and the Audio signal is muted when the channel is changed or when the Mute key is pressed. When the set is turned On, the last channel viewed is tuned in. If power is interrupted, the system tunes to channel 3.

The tuning section selects channels by four methods: Remote Control Channel Scan, Remote Con- trol Random Access, On-Set Channel Scan, and On-Set Random Access. The system selects the RF input signal desired from the RF Switcher, searches for offset carriers (in the Cable mode), and provides Automatic Fine Tuning control for the Tuner.

The major components on the Tuner Interface Panel are: Serial-to-Parallel Converter IC1, IF Module, Video Buffer Q9, Audio/Video Switching Transistors Q5/Q6/Q7/Q8, DC Control Buffers Q14/Q15/Q16/Q17, Vertical Blanking Amp- lifiers Q21/Q18, Coincidence Detector Q3/ Q4, Color Video buffers Q10/Q11/Q12, Fast Blank- ing Inverter Q13, Relay Control Transistors Q19/Q20, and 60Hz Clock Amplifier Q2.

The Serial-to-Parallel Converter IC1 receives serial data from the Microcomputer at Pin 8, after the Microcomputer has been addressed, and the data is clocked in when IC1-5 is enabled. Parallel data at IC1-20, -21, -23, -24 drive inverters, which individually feed the Input/ Output Panel J715. Active Lows are required by the RF Switcher at J52 from IC1-16, -14, -13 to switch the RF inputs in sequence. The Tuner Interface Panel also couples switching signals and tuning voltages to the Tuner. Hi/Lo VHF Bandswitch voltages from CITAC are fed through the Controller P37-17 to the Tuner via J11-17 and J8-4, while the Superband switching voltages are fed through J11-18 and J8-2. The Tuning voltage is output through J11-15 and exits the Tuner Interface Panel through J11-14 and J9-4.
Other functions of the Tuner Interface Panel are: control lines to the Stereo Power Amplifier for Bass control J-11-6/J10-1, Treble control

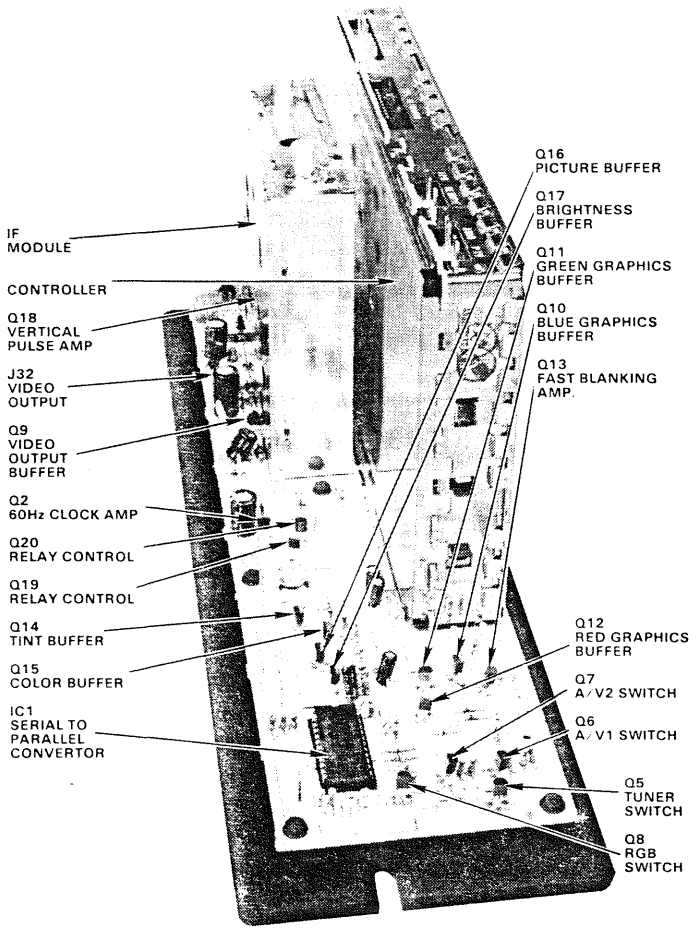


Figure 12 — TS-10P Tuning System Assembly

Graphics Generator on the Controller. Composite Blanking is developed by adding Vertical pulses to the Horizontal pulse line through Inverter Q21. Blanking is then coupled to the Graphics Generator on the Controller. R, G, and B Graphics Video signals are fed through RGB Buffers Q12, Q11, and Q10 to the Video Processor Panel J414 through J18-1, -2, and -3. Fast Blanking pulses are fed to the Input/ Output Panel through J18-4. Composite Sync and -70 Volt pulses are fed through J11-2, -8 to the Coincidence Detector Q3/Q4 and the output voltage is applied to the Controller. The Relay Switch Q19 and Q20 are driven from the Controller and provide a Low (ground) for the Power Relay RY1 coil through J2-3. The 60Hz Clock Amplifier Q2 is driven from J2-1 and supplies 60 Hz timing pulses to the Microcomputer J11-19.

J11-7 / J10-3, Balance control J11-9/ J10-5, and Volume control J11-2/J15-1; inputs to the Controller J29-3/J11-4 and J29-1/J11-3 for Stereo and SAP program recognition; and control line inputs, buffers, and outputs for Picture Preference adjustments for Tint J5-1/ Q14/J4-1, Color J5-2/Q15/J4-3, Picture J5-4/Q16/J6-5, and Brightness J5-5/Q17/ J6-4.

The IF Module outputs AFT voltage to the Controller through J11-8. The Composite Video signal is output from J7-5, buffered by Q9, and output at J32. AGC voltage is fed to the Tuner through J9-1, and Audio is output to the Stereo/SAP Decoder J26 from J31-1.

Vertical and Horizontal pulses are fed through J1-6, -5 and J11-28 to synchronize the

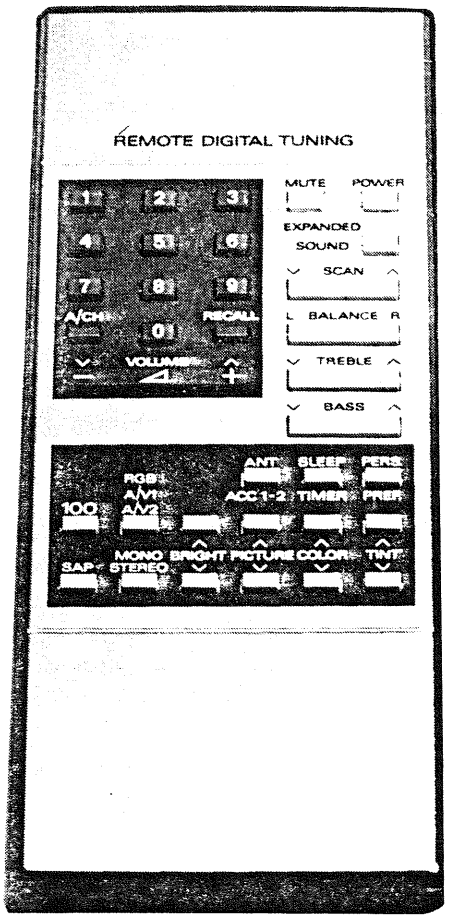


Figure 13 - 40-Button IR Remote Transmitter

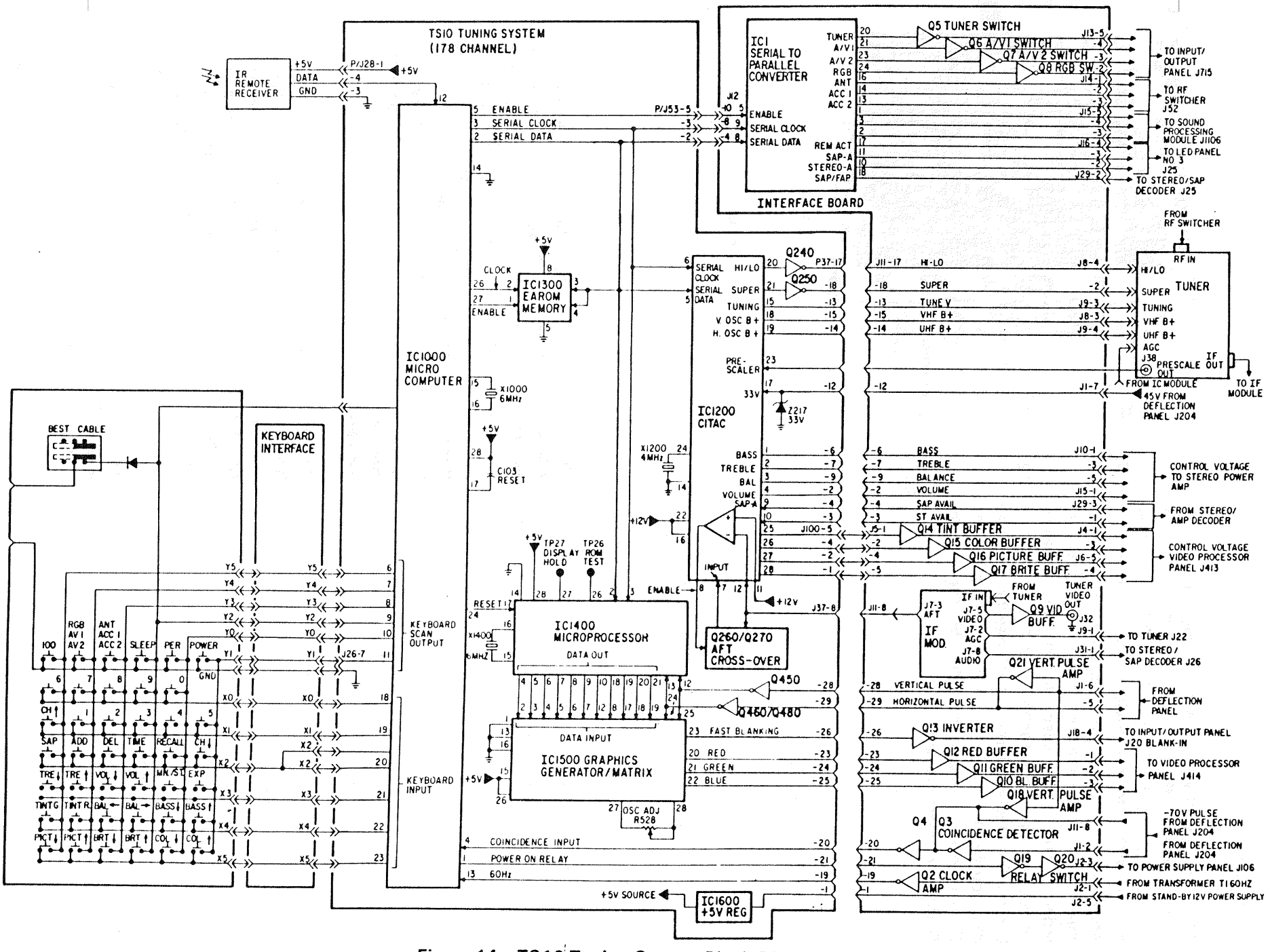


Figure 14 - TS10 Tuning System Block Diagram

RF Switcher

The RF Switcher, shown in **Figure 15**, is located between the RF input connection to the set and the input to the Tuner. Three RF signals may be connected to the Switcher input jacks. In addition to the signal from the VHF TV antenna, the RF signal from accessories such as VCRs, video games, video disc players, and personal computers can be attached. At the press of a button, the desired input signal can be selected and coupled to the Tuner. The small size of the RF Switcher is made possible by the use of Surface Mounted Devices.

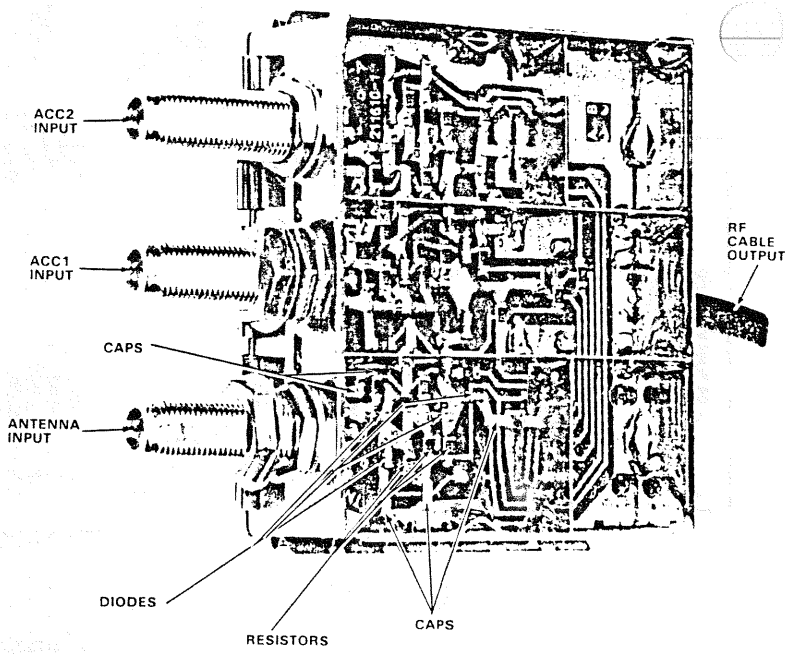


Figure 15- RF Switcher

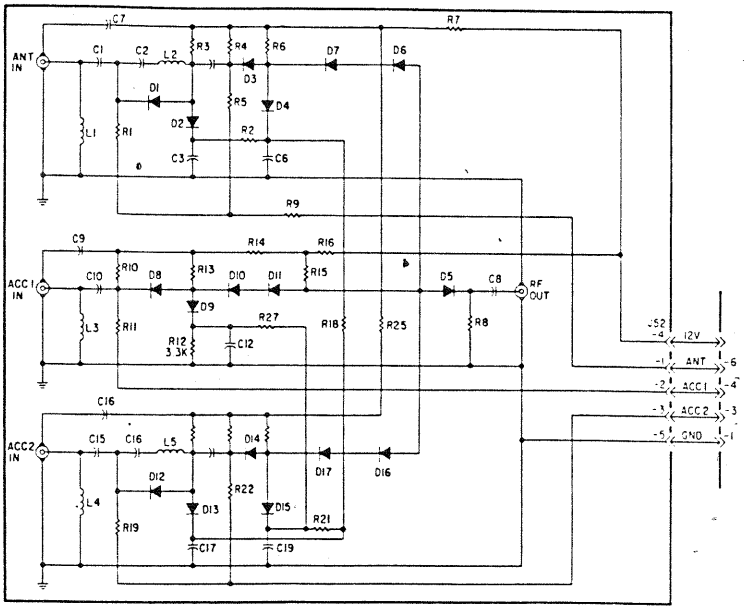


Figure 16- RF Switcher Circuit

The circuitry of the RF Switcher is shown in **Figure 16.** When the Power button is pressed, the Microcomputer IC1000 program selects the RF Switcher Antenna input. IC1000-22 turns On Q340 with a logic High to provide a ground through CN1300-6 and RF Switcher J52-1 for the switching diodes. the switched-On diodes D1 and D3 couple the RF signal from the antenna input jack through D7, D6, and D5 to the RF output cable.

The RF input signal from Accessory 1 (ACC1) or Accessory 2 (ACC2) is selected with the Tuning Keyboard RF button. Pressing the RF button once advances the RF Switcher to the next position. IC1000-23 logic High turns On Q342, which supplies an active load to RF Switcher J52-2 from the Controller CN1300-4. The On Diodes D8, D10, D11, and D5 pass the ACC1 RF signal to the RF output. Pressing the RF button again selects ACC2. IC1000-24 logic High turns On Q344. The active Low fed to RF Switcher J52-3 from CN1300-3 turns On diodes D12, D14. The ACC2 RF signal is fed through the conducting diodes to the Tuner.

IF Module

The IF Module shown in **Figure 17** plugs into the Tuner Interface Panel. Callouts point to the major components and adjustments. the Video IF Input jack, J1, is shown in the upper left portion of the diagram. Located to the right: L2 47.25MHz Adjacent Channel Sound Trap, F1 Saw Filter, Q1 IF Pre-Amp, IC1 Video IF/Detector, L6 and L7 respectively, Q3 Equalizer, and the Input/Output connector J10. To the left: Q4 Video Output, AGC Adjust VR7, IC2 Sound Detector, L16 45.75MHz Detector Coil, and L12 4.5MHz Discriminator.

As seen in **Figure 18**, the IF cable from the Tuner is connected to the If Module at J1. The Adjacent Channel Sound signal is trapped at 47.25MHz by C1/L2; then, the signal is amplified by Q1 and fed to SAW Filter F1, where two bandpass curves shape the Video IF and Sound IF responses. The Video response is notched at the 41.25MHz Sound carrier and fed to IC1 for amplification detection. After detection, the Video signal is passed through a 4.5MHz trap to remove all traces of the sound carrier. About 2Vpp Sync-negative, Composite Video is output from Q4 to the Tuner Interface Panel and through Video Buffer Q15. The buffered Video is fed to the Input/Output Panel.

The second response of the SAW Filter suppresses Video sidebands and passes the Video and Sound IF carriers. The two carriers drive IC2, which detects the 4.5MHz difference signal, or Sound carrier. The Sound carrier is amplified, limited, and quadrature detected into wideband Audio. The Audio output signal, with an amplitude of about 0.5 volts RMS, is coupled to the Stereo/SAP Decoder.

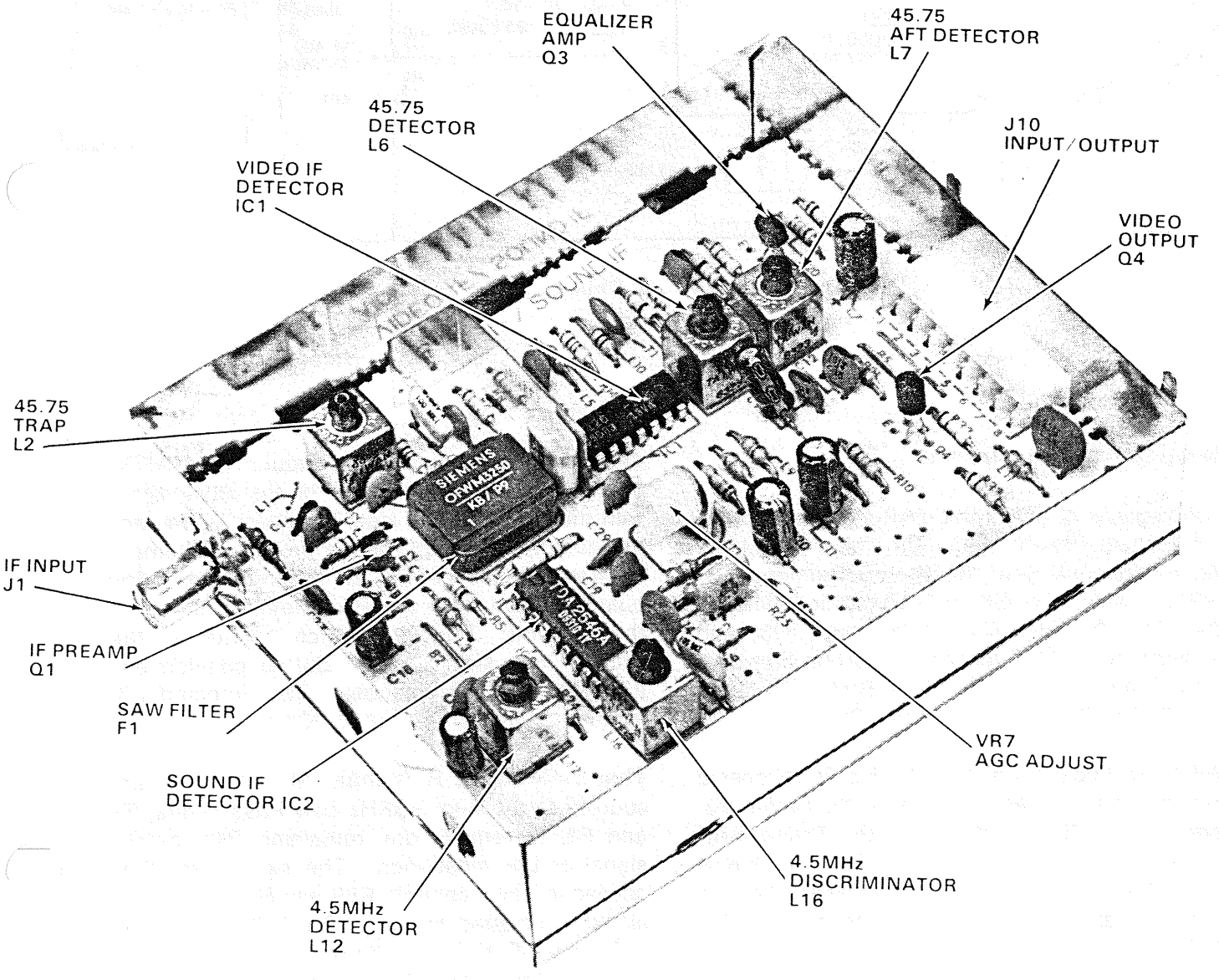


Figure 17 - IF Module

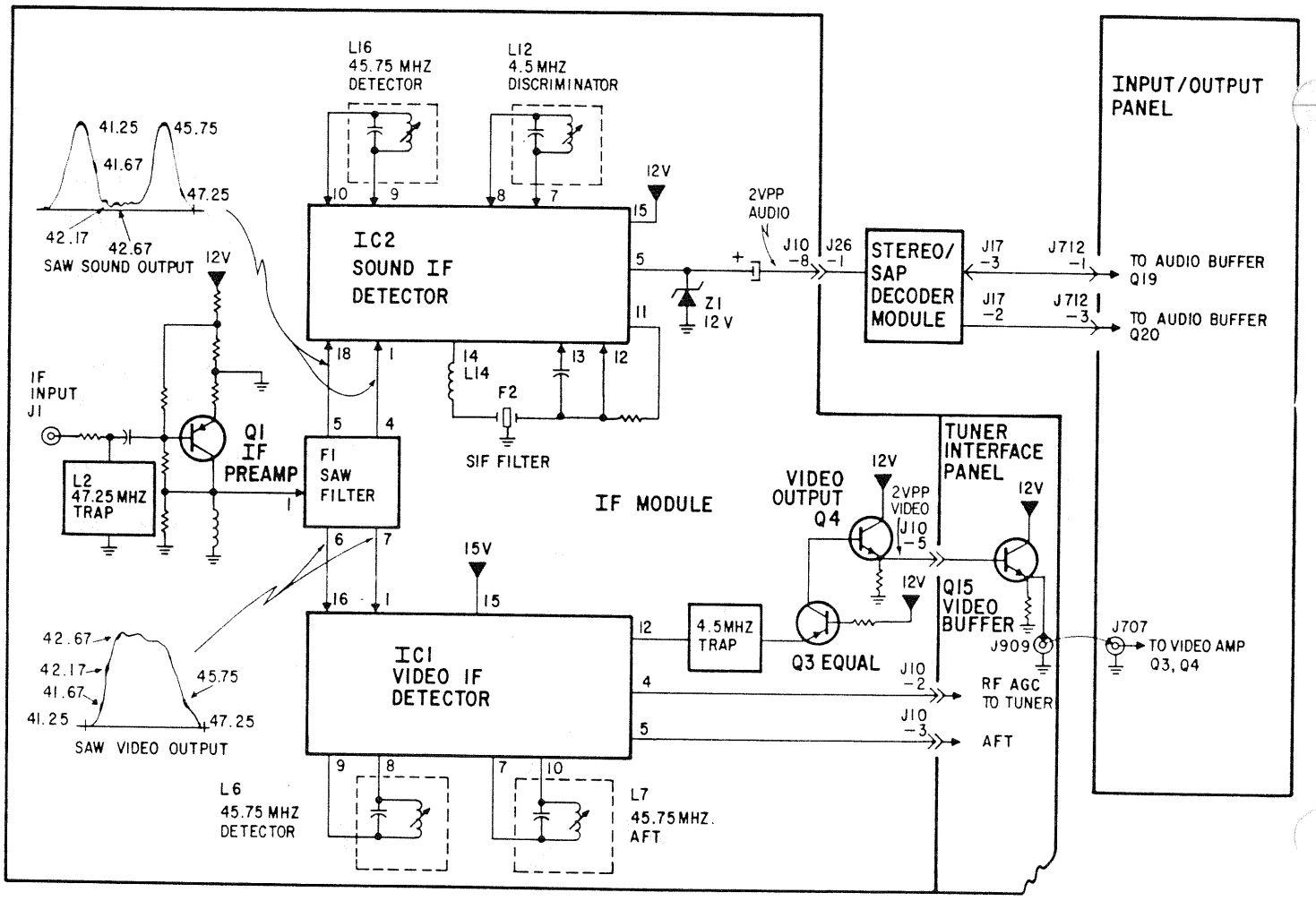


Figure 18 - IF Circuit

Stereo/SAP Decoder Module

A photograph of the Stereo/SAP Decoder Module is shown in **Figure 19.** The major functions and components are: the Stereo Decoder IC1, L+R/L-R Amp IC4, Stereo/SAP Audio Switches IC6, SAP Decoder IC2, Comparator IC3, and Expander IC5. The transistor functions are: SAP Audio Amp/-Mute Q3, All Pass Buffer Q4, High Pass Buffer Q5, and -L+R Buffer Q6.

Wideband Audio (to about 100KHz) is recovered from the Sound Detector and fed to the Stereo Decoder IC1-1, **Figure 20**, where the 79KHz SAP Pilot signal is trapped by C2/L1. The L+R signal is buffered and output at Pin 4, while the L-R signal is applied to the L-R Decoder. The 15.734KHz Pilot carrier is buffered and applied to the Pilot Detector and the Automatic Frequency and Phase Control (AFPC) circuit. The AFPC circuit compares the phase of the Pilot signal with the phase of the local Oscillator signal, and the output correction voltage provides automatic frequency/phase control for the oscillator. The output voltage from the Pilot Detector turns On the Schmitt Trigger, which switches the Stereo/Mono switch to the Stereo position and turns On the L-R Decoder. The detected L-R signal is buffered and output IC1-5.

The L+R and L-R signals at IC1-4, -5 are coupled to the 0-to13.5KHz Low Pass Filters, F3 and F2, to remove any remaining Pilot carrier signal or L-R sidebands. The signals are then applied to Level controls R58 and R50. The L+R signal is coupled to the L+R/L-R Amps in IC4, while the L-R signal is coupled to the "Y" switch, IC6-3. When the SAP switch is in the Off

position, the "Y" switch is closed and connects the L-R signal to Pin 4. The L-R signal is coupled through Buffer Q4 to Pin 18 of the Expanded IC5. This signal is also passed through a 100Hz-to 3KHz Bandpass Filter to IC5-3 and through Q5 Buffer and a 4KHz-to 9KHz Bandpass Filter to IC5-20.

During the original encoding process at the transmitter, the amplitude of the L-R Audio frequencies within the passbands is reduced, or "compressed," as part of a scheme to improve the overall signal to noise ratio. The variable reduction of the dynamic range for the low and middle Audio frequencies permits a higher average level of modulation at the transmitter, which masks most of the noise introduced in the remaining part of the system. To restore the L-R signal to its original proportions, the same bands of frequencies are amplified, or "expanded," by the same amount as they were compressed in the encoding process. IC5 performs the "expander" function. the Audio signal for the SAP channel goes through the same compression-expanding or "companding" process.

The 0-to-13.5KHz L-R signal is fed to the variable Gain Amp "B," and the 4KHz-to-9KHz band of frequencies is coupled to RMS detector "B." A variable dc voltage is developed by the detector which is proportional to the average level of the Audio frequencies within the passband. This control voltage is applied to Variable Gain Amp "B." The amplitude of the L-R signal at Pin 17 is "expanded" in direct proportion to the variations of the dc control voltage. The signal is amplified by Output Amp "B," amplified and inverted by Op Amp "B" in IC4, and coupled back through IC5-5 to Variable Gain Amp "A." A similar action takes place here that occurred in Amplifier "B," except the variable dc control voltage is developed from the 100Hz-to-3KHz band of frequencies. the previously expanded L-R signal is expanded again in direct proportion to the average level of the Audio frequencies with this lower passband. the relative amplitude of the L-R Signal is now identical to the original L-R signal, but with an improved signal-to -noise ratio. The signal is amplified and inverted by output Amp "A" and exits Pin 8 as a -L+R signal. The -L+R signal is buffered by Q6 and applied to the resistor network at the inputs of Op Amp "C" and "D." Right Audio is recovered

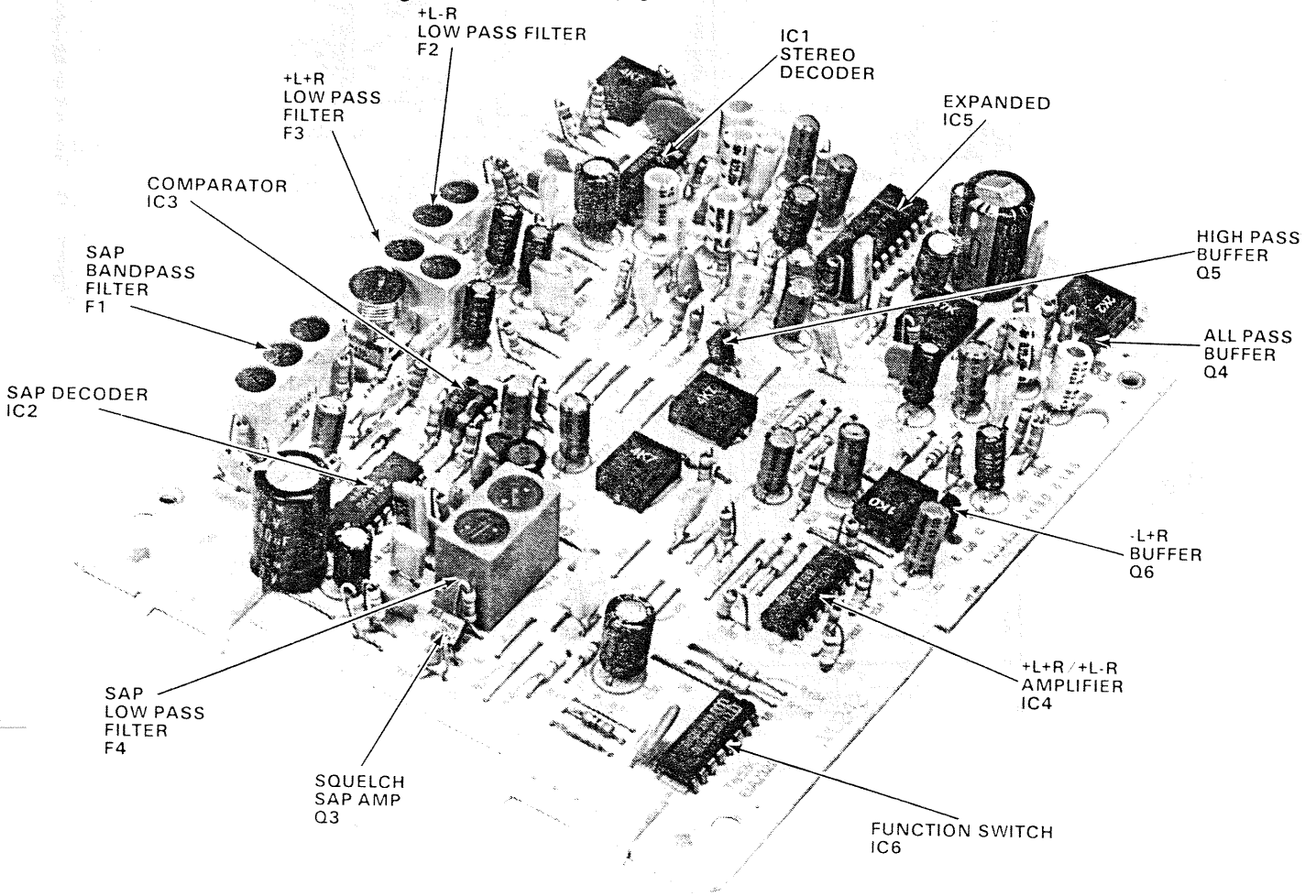


Figure 19 - Stereo/SAP Decoder Module

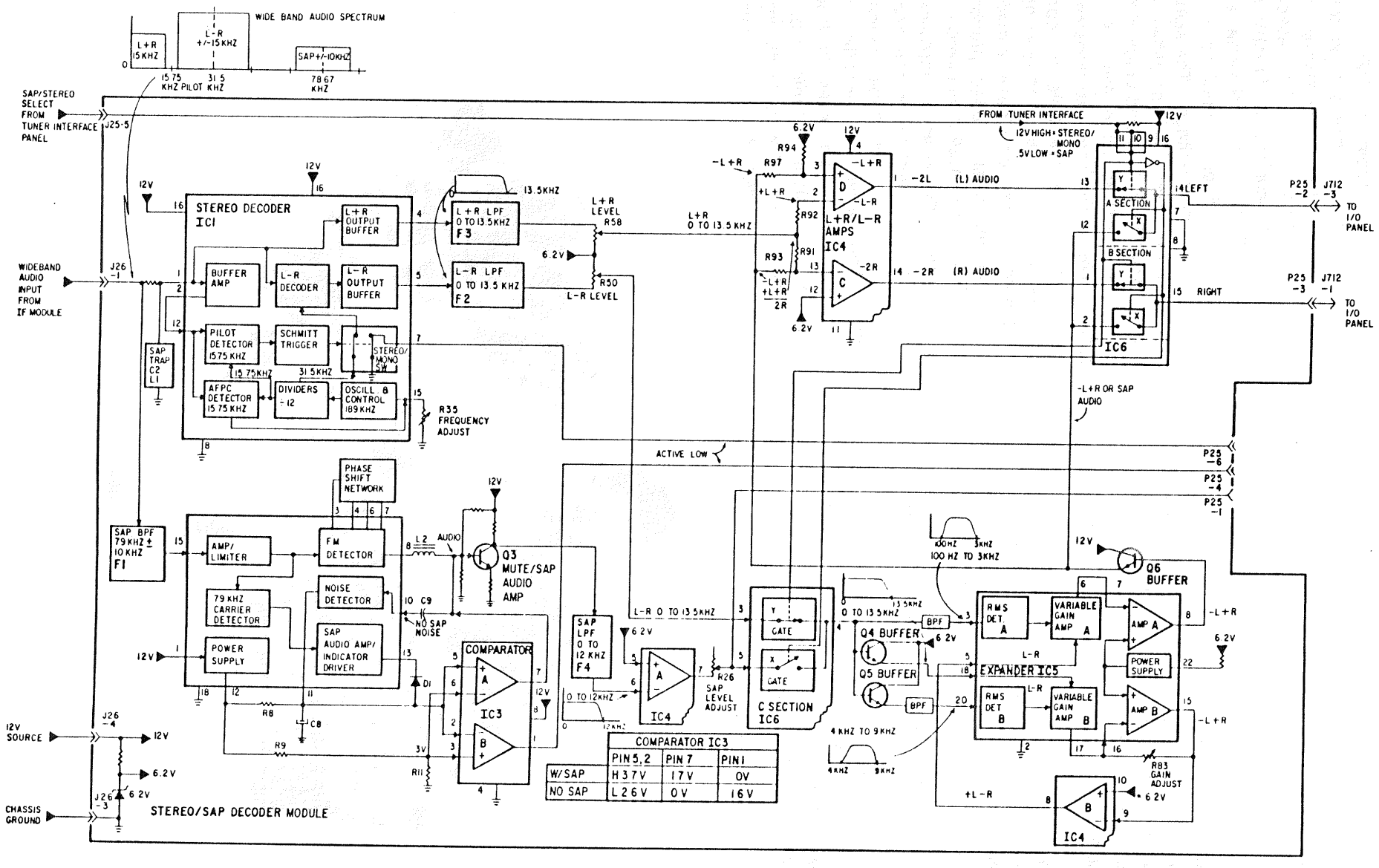


Figure 20- Decoder Module Signal Flow Diagram

in resistor matrix R93/R91. When the +R+R and -L+R signals are added, the opposite polarity L signals cancel, while the two positive R signals add. The 2R signal is applied to Pin 13, the inverting input terminal of Op Amp "C," and appears in the output at Pin 14 as -2R.

The Left Audio is recovered in a slightly different manner in Op Amp "D." The -L+R signal is applied to the non-inverting input Pin 3 while the +L+R signal is applied to the inverting input Pin 2. In this case, the -L+R signal remains -L+R in the output while the +L+R signal is inverted to -L-R. The opposite-polarity R signals cancel which allows the in-phase -L signals to add to -2L. the Right and Left Audio signals are coupled to the inputs of the "Y" switches IC6-1, -13 respectively.

The electronic switches in IC6 are controlled by a dc voltage applied to Pins 9, 10, and 11. When this voltage is High (12Vdc), all three "Y" switches are turned On and the three "X" switches are turned Off. Conversely, when the control voltage is Low (0.5Vdc) the "Y" switches are turned Off and the "X" switches are turned On. (The "X" switches are closed only when the SAP switch is in the "SAP" position.) With the "Y" switches closed, the Left and Right Audio signals are couples to the Input/Output Panel.

The wideband Audio signal from the Sound Detector is fed to the SAP Bandpass Filter F1, which passes the SAP signal band of frequencies from 69KHz to 89KHz to the SAP Decoder at IC2-15. When a second Audio Program is transmitted, the signal is amplified and limited. the 79KHz SAP carrier is applied to the 79KHz Carrier Detector, which outputs a control voltage to the SAP Audio Amp/Indicator Driver. An active High is output Pin 13 which reverse biases D1. A positive voltage provided by the internal power supply at Pin 12, is applied through R8 to the non-inverting input Pin 5 and the inverting input Pin 2 of IC3. This voltage exceeds the fixed 3Vdc on Pin 3 and provided by divider resistors R9 and R11. The High on Pin 5 produces a High at Pin 7 which turns on Q3, the SAP Audio/Mute Amplifier.

The SAP FM signal is detected by the FM Detector. The SAP Audio signal is output at Pin 8 and amplified by Q3. The signal is then passed through a 0-to-12KHz lowpass filter to Pin 6 of IC4. The amplified SAP signal is output Pin 7, taken from the arm of the Level Adjust control, and applied to the "X" switch input Pin 5 of IC6. If the SAP switch on the Control Panel is activated, the "X" switches close and the "Y" switches open. The SAP signal is processed in the Expander IC, buffered by Q6 and applied to Pins 2 and 12 of IC6. the monaural SAP signal is then coupled through the closed "X" switches to both Left and Right Audio channels.

If the SAP Audio signal becomes noisy, such as during weak signal conditions, the high frequency noise couples through C9 to the Noise Detector. the output at Pin 11 switches IC3-5 and -2 Low. the Low at IC3-7 cuts Off Q3 and prevents the noise from reaching the following Audio circuits. the High at IC3-1 turn Off the SAP indicator by opening the return lead. If a SAP Signal is not transmitted at all, there is no output from the 79KHz Carrier Detector. The output from the SAP Audio Amp/Indicator Driver, Pin 13, places a Low on IC3-2 and -5. Pin 7 goes Low and cuts Off (mutes) Q3.

Tuner Interface Panel

The block diagram of the Tuner Interface Panel, **Figure 21**, shows four and five button keyboards interfacing with switching circuits. The four button Audio/Video Keyboard selects one of the four program sources; Tuner Audio/Video, A/V1, A/V2 or RGB Audio/Video. The five-button Sound Processing Keyboard selects on the the five Audio modes: monaural, stereo, monaural or stereo expanded, or SAP. Each of these switching circuits outputs a 0/12Vdc voltage which switches the Audio and/or Video signals on the Input/Output Panel, and selects the appropriate operating mode of the Sound Processor Module.

The circuits on the IF Module develop AFT and AGC voltages for the Tuner and detect the Composite Video signal and the Audio signal. The Video signal is coupled to the Input/Output Panel and the Audio signal is applied to the Stereo/SAP Decoder Module. Horizontal pulses from the Deflection circuit are applied to a Coincidence Detector. When a TV channel is selected, the Composite Sync pulses appear only when the station is tuned in. When "coincidence" occurs (when the Flyback pulses and Sync pulses are in phase), the detector outputs a voltage to the

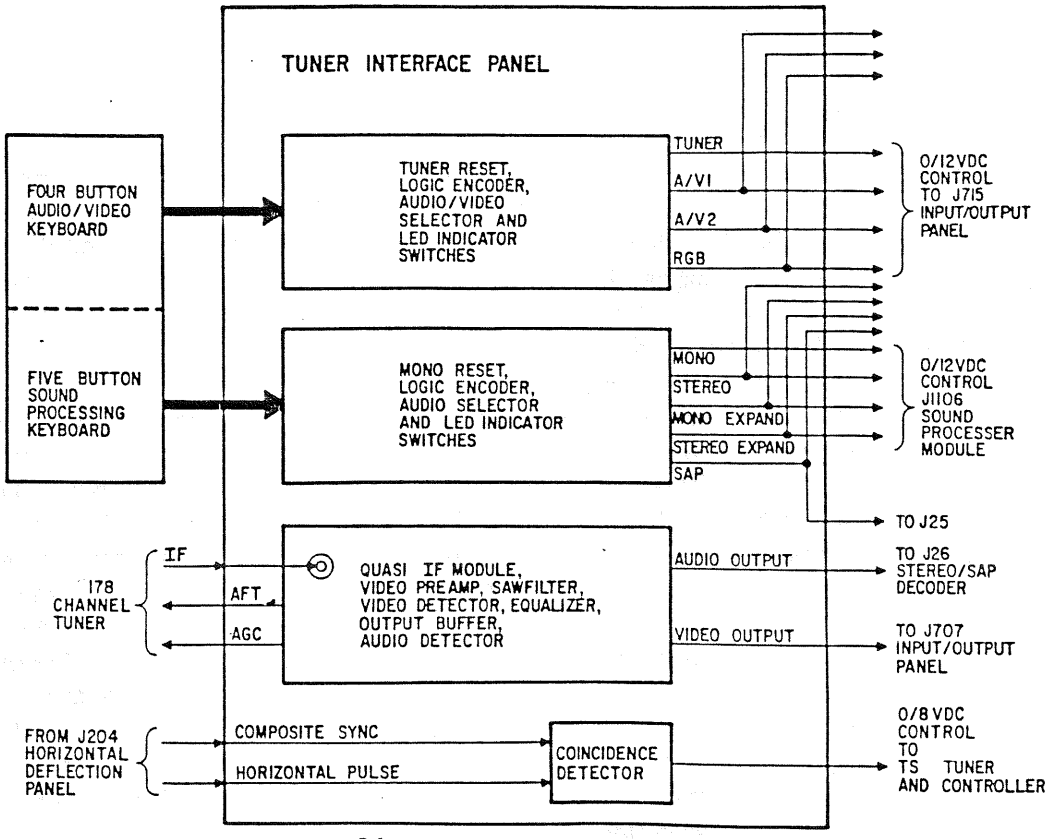


Figure 21 - Tuner Interface Panel Block Diagram

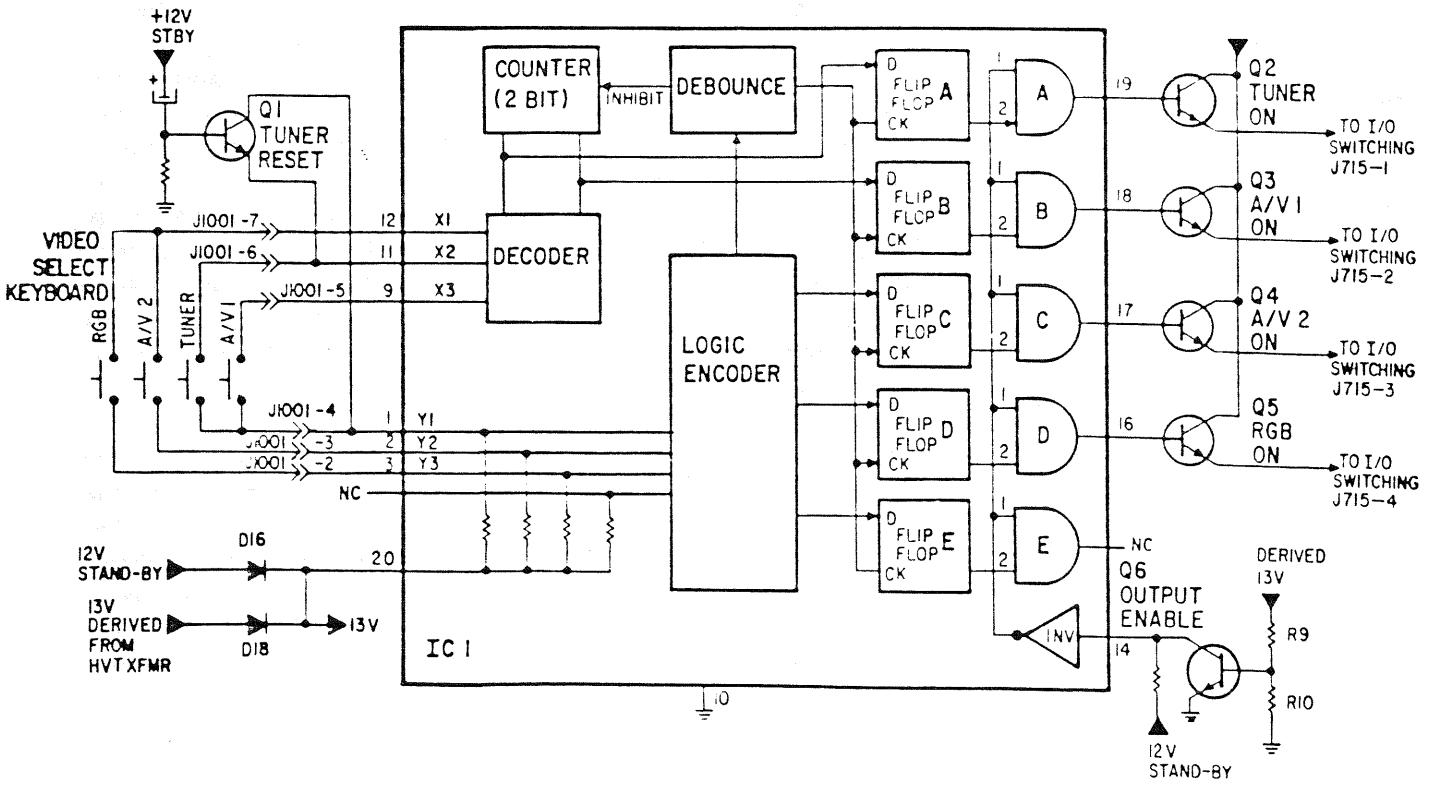


Figure 22 - Audio/Video Logic Encoder

tuning control system to stop the tuning action.

The Tuner Interface Panel Audio/Video Logic Encoder section, **Figure 22**, shows the Audio/-Video Select Encoder IC1, Video Select Keyboard, and Tuner Reset transistor Q1. Also shown are dc switching transistors Q2 through Q5, which control electronic switches on the Input/Output Panel that select the Audio/Video signals from the Tuner, A/V1, A/V2 or RGB inputs. The Output Enable transistor Q6 places a High on Pin 1 of AND Gates A through E continuously when the set is in operation.

When AC power is first applied to the set, the 12Vdc Stand-By voltage turns on Q1 momentarily and shorts IC1-1 to IC1-11. The active Low is decoded and fed to Flip Flop A, which outputs a High to AND Gate A input 2. Pull-up resistor R8 holds IC1-14 High at 12Vdc, which is inverted to a Low and fed to AND Gate A input 1. The output of AND Gate A remains Low and Q2 is turned Off. When the Power button is pressed and the scan-derived dc voltages develop, Enable Q6 is turned On by 13Vdc applied to the bias network R9/R10. Q6 On condition pulls IC1-14 Low. Internally the Low at Pin 14 is inverted to a High and applied to Pin 1 of all AND Gates. With both inputs of AND Gate A High, the output at IC1-19 is High and turns On Tuner switch Q2. The tuner switch outputs an emitter High to Input/Output Panel J715-1 from J911-5 to be used as the control voltage for the Tuner Video and Audio Switching.

Input/Output Panel

The Input/Output Panel, or I/O Panel, is shown in **Figure 23**. Five bilateral switch ICs, containing four switches each, switch the selected Audio and Video signals to their respective output circuits. Switching logic from the Tuner Interface Panel selects Audio and Video signals from the internal TV Tuner (Video Detector and Sound Detector outputs), external Audio/Video inputs A/V1 or A/V2, or the RGB inputs. All Video input and output jacks are terminated with 75 Ohm resistors when the Bridge/Terminate switch is placed in the Terminate position. When this switch is in the Bridge position, the 75 Ohm resistor is removed and the Video signal connected to the input jack loops through and must be terminated by a

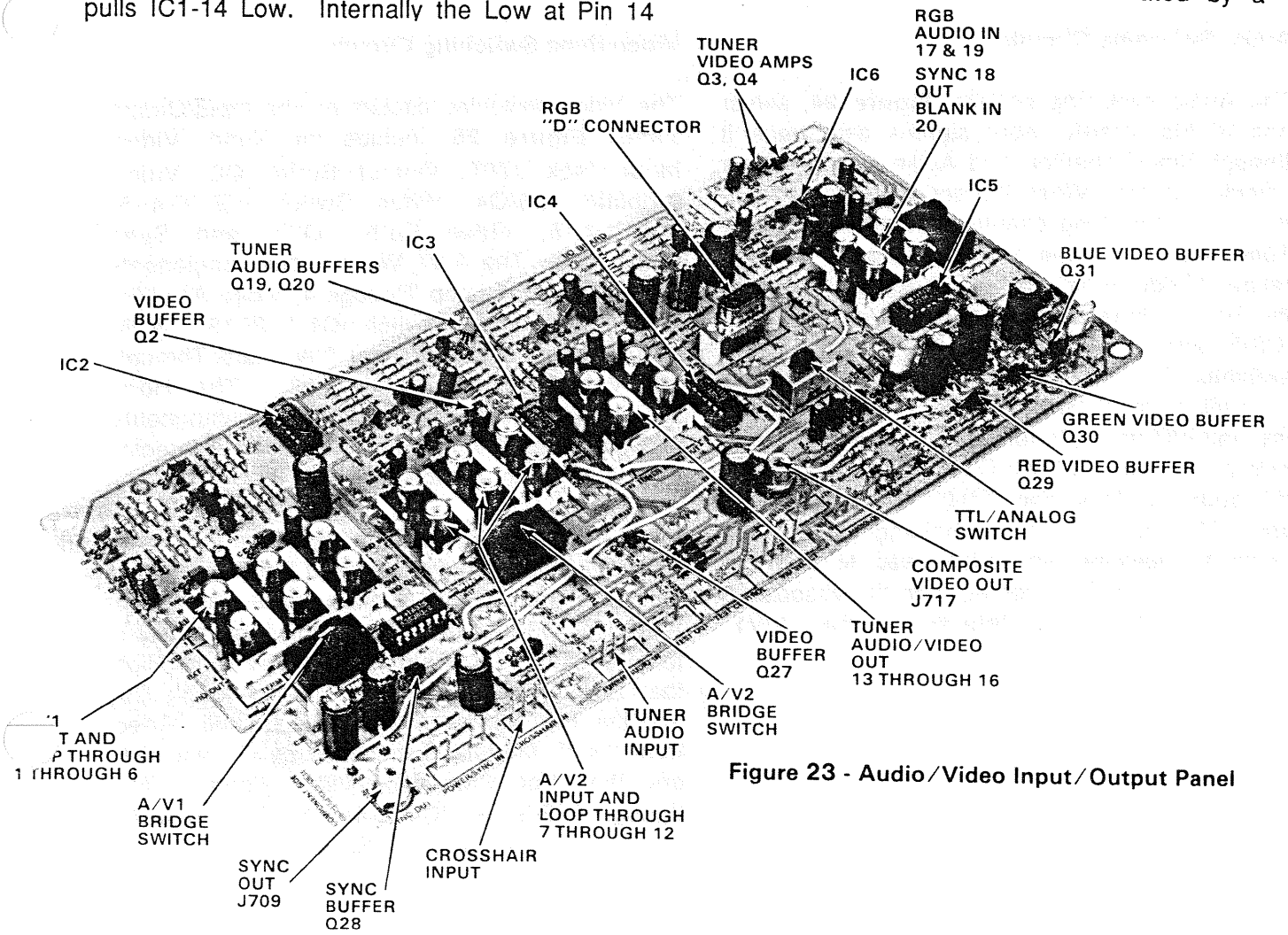


Figure 23 - Audio/Video Input/Output Panel

monitor, VCR, or other accessory at the end of the Video cable. RGB Video from either a TTL (digital) or analog source is terminated by the TTL/Analog switch. TTL Video is terminated by a 2.2K Ohms load impedance and an analog signal is terminated into 75 Ohms. The Audio sources are terminated with a 47K Ohm resistor.

Other signal inputs to the I/O Panel are: Crosshair Video, Horizontal and Vertical Sync, and Fast Blanking. Crosshair Video, generated on the Convergence Panel, is fed to J713-1 and switched into the Video circuits with the Test/Normal switch SW1 (on the Control Panel). Crosshair Video is coupled through IC4-1, -2, Video Buffer Q27, to the Comb Filter J501. Sync correction is automatic for either digital or analog RGB Video signals connected into the "D" connector. If the signal pulses have the wrong polarity or if the pulses are distorted, Q18 and IC6 reshape the pulses and correct the polarity. If Sync pulses are good and the polarity is correct, the circuit passes the signal without correction, through IC3-8, -9, Q28, and output jack J709 to the Horizontal Oscillator Module input jack J302.

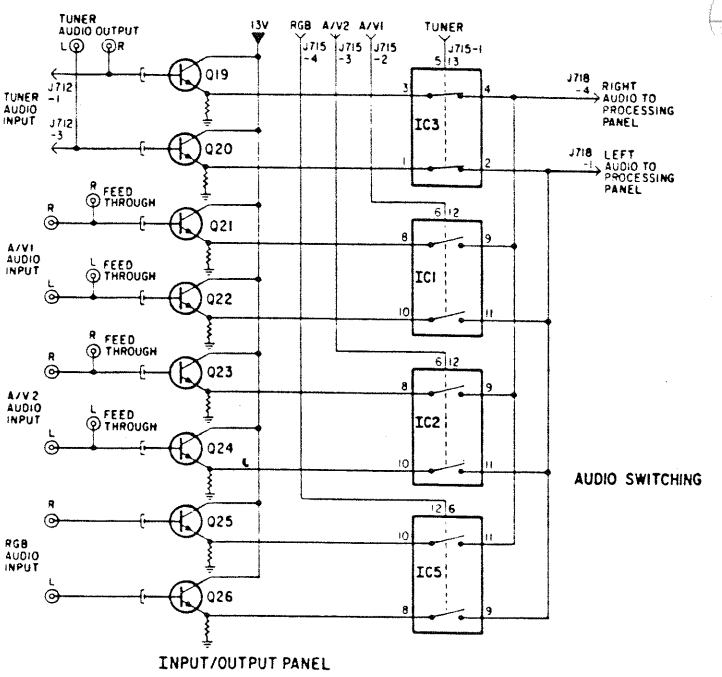


Figure 24 - Audio Switching Circuit

Audio Switching Circuits

The Audio switching circuits, **Figure 24**, select one of four stereo input signals and feeds it through input preamps and Audio switches to a common output. When the set is first turned On, the Audio switching circuits automatically select Tuner Audio and the Monaural mode. A High (about 12Vdc) is fed to the I/O Panel J715 from the Tuner Interface Panel. The 12Vdc applied to IC3-5 and -13 turns On the Tuner Audio switches IC3-3 to -4 and IC3-1 to -2. Decoded TV Audio from the Stereo Decoder Module is fed to the Input/Output Panel J712-1 and -3. It is then buffered by Q19 and Q20 and switched to the I/O output J718-4 and J718-1 by IC3-3 to -4 and IC3-1 to -2. The remaining circuits are identical; however, the High used to turn On other Audio switches comes from the associated switch on the Tuner Interface Panel, A/V1, A/V2, or the RGB switches.

Video/Sync Switching Circuits

The Video switching circuits on the Input/Output Panel, **Figure 25**, include the Tuner Video Input Jack J707, Output Buffer Q2, Video Amplifier Q3/Q4, Video Switch IC2-3/-4/-5; IC4-3/-4/-5, Video Buffer Q27, and Sync Buffer Q28. The A/V1 Video circuit components are: Input 1 and Loop Through 4, Video Amplifier Q7/Q8, and Video Switch IC1-1/-2/-13. A/V2 circuit components are: Input 7 and LoopThrough 10, Video Switch IC2-1/-2/-13. The Horizontal and Vertical RGB Sync circuit components are: the Clamp Amplifier Q18, Sync Corrector IC6, and Sync Switch IC3-8/-9/-6.

When the set is turned On, a High from the Tuner Interface Panel is developed and fed to the Input/Output Panel J715-1, which turns On Video Amplifiers Q3 and Q4. The same High at IC2-5 turns On IC2. IC4 is turned on by the same High that is fed to IC4-5 from J715-1 through D9, and the Test/Normal Switch SW1. Tuner Video from the IF Module is amplified by Q3 and Q4, and the 1Vpp Composite Video signal is fed through IC2-3, -4, IC4-3,-4, and Q27 to J717 output and on to the Comb Filter.

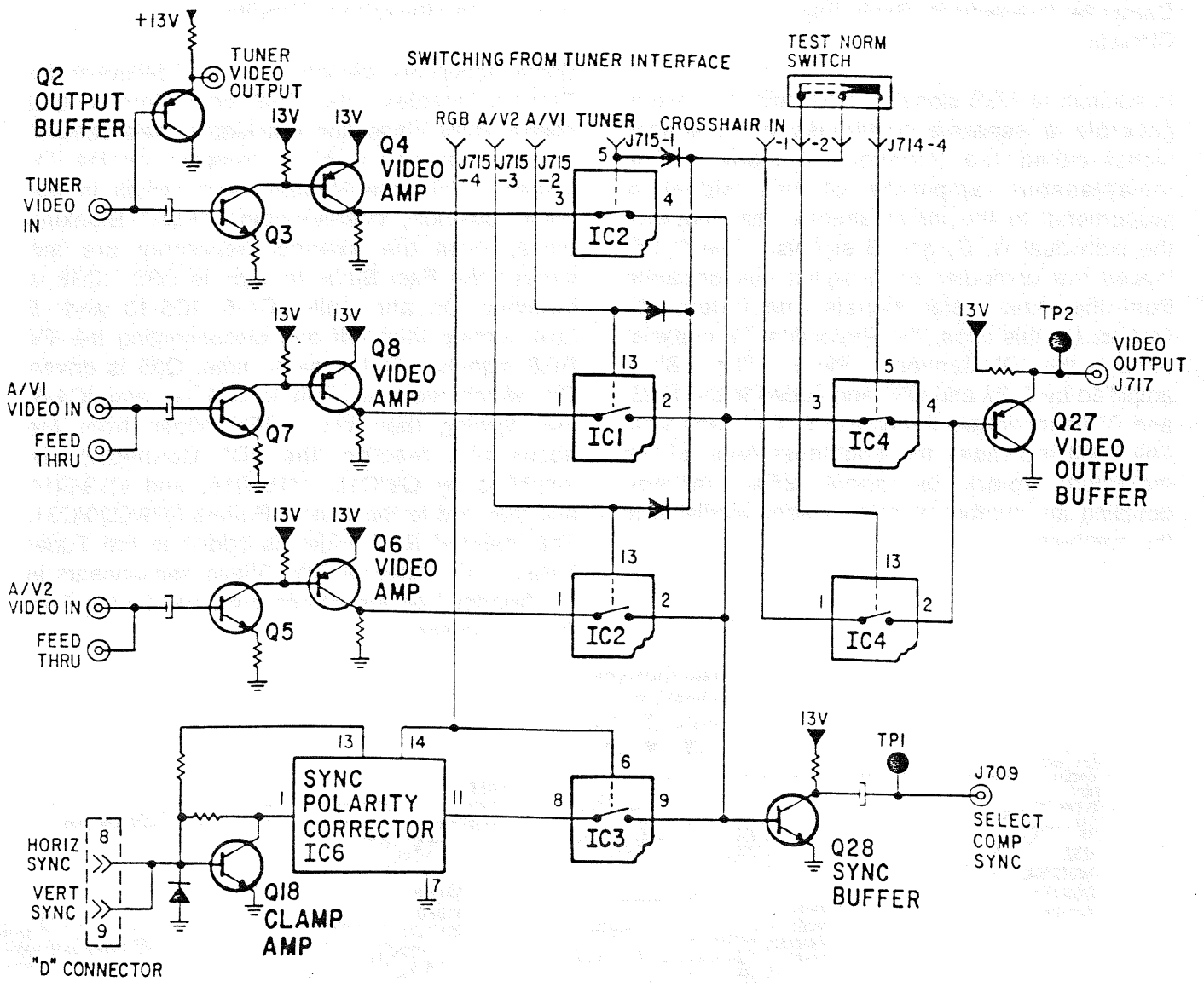


Figure 25 - Video/Sync Switching Circuit

RGB Switching Circuits

Figure 26 shows the major functions and components of the RGB switching circuits: RGB Input Jacks J708/J706/J705, Fast Blanking In Jack, IC1-3/4/5 Red Video Switch, IC5-1/2/13 Green Video Switch, IC5-3/4/5 Blue Video Switch, Q29 Red Video Buffer, Q30 Green Video Buffer, Q31 Blue Video Buffer, Red/Green/Blue Video Output Jacks J703/J702/J701, "D" Connector Red/Green/Blue Input Q9/Q10 Red Video Amplifier, Q15/Q16 Green Video Amplifier, Q13/Q14 Blue Video Amplifier, Q34/Q33 Intensity Bit Amplifiers, Q32 Internal RGB Switch, Q33 External RGB Switch, and Normal/Insert Switch SW4.

RGB Amplifiers Q9/Q10, Q15/Q16, and Q13/Q14 are biased On all of the time by 13Vdc fed to the bias networks by diodes D5,D8, and D7. The Normal/Insert switch SW4, when in the Normal position turns on the RGB Video switches by connecting 13Vdc to control pins IC3-12,IC4-6, and -12. Also they can be turned On by Q35 collector voltage when SW4 is in the Insert position and program Blanking is present. When Insert and Tuner, A/V1, or A/V2 are used, Video Switches IC1-/3/4/5, IC5-1/2/13, and IC5-3/4/12 are On and feed selected Video to their Output Buffers.

Computer Intensity Bit Switching Circuits

In addition to RGB signals, some color computers generate a separate brightness or luminance signal called the Intensity Bit signal. The instantaneous amplitude of this signal is proportional to the instantaneous amplitude of the individual R, G, and B signals. The "I Bit" leaves the computer on a signal line separate from the three color signals and enters the monitor (in this case, the Projection TV chassis) through the "D" Connector Pin 6. The I Bit is amplified by Q 34 and Q33 and added to the R, G, and B Video signals through D19, D17, and D18. The I Bit increases the brightness level of the individual colors by about 25%, thereby doubling the number of color shades available to the computer.

Insert Video Switching Circuits

Some accessory devices such as decoders for Teletext/Videotext and RGB computers, output special RGB Video and Blanking signals used to insert information within a "window" on the TV screen. With the Normal/Insert switch in the insert position, positive-going "Fast" Blanking pulses from the external accessory are fed through the Fast Blank In Jack to Q32. Q32 is switched On and pulls IC1-5, IC5-13 and -5 Low, turning then Off and disconnecting the TV RGB signals. At the same time, Q35 is driven Off, which feeds a High to IC3-12, and IC4-6, -12, turning then On. RGB Video from the accessory, feeding the "D" Connector, is amplified by Q9/Q10, Q15/Q16, and Q13/Q14 and then fed to the Output Buffers Q29/Q30/Q31. The Inserted RGB Video is added to the Tuner Video, A/V1 Video or A/V2 Video and appears in the "window" on the screen produced by the Fast Blanking pulses.

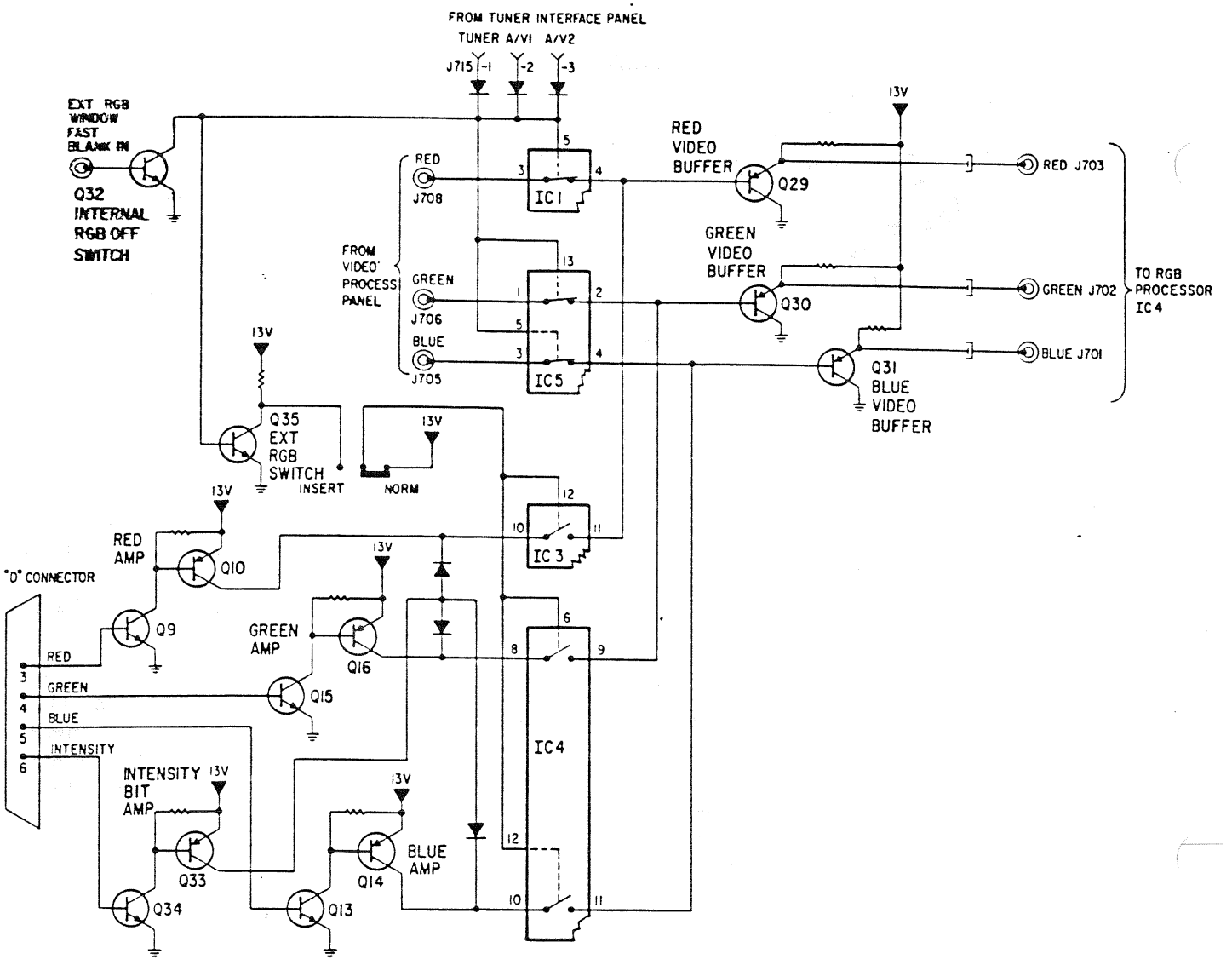


Figure 26 - RGB Video Switching Circuit

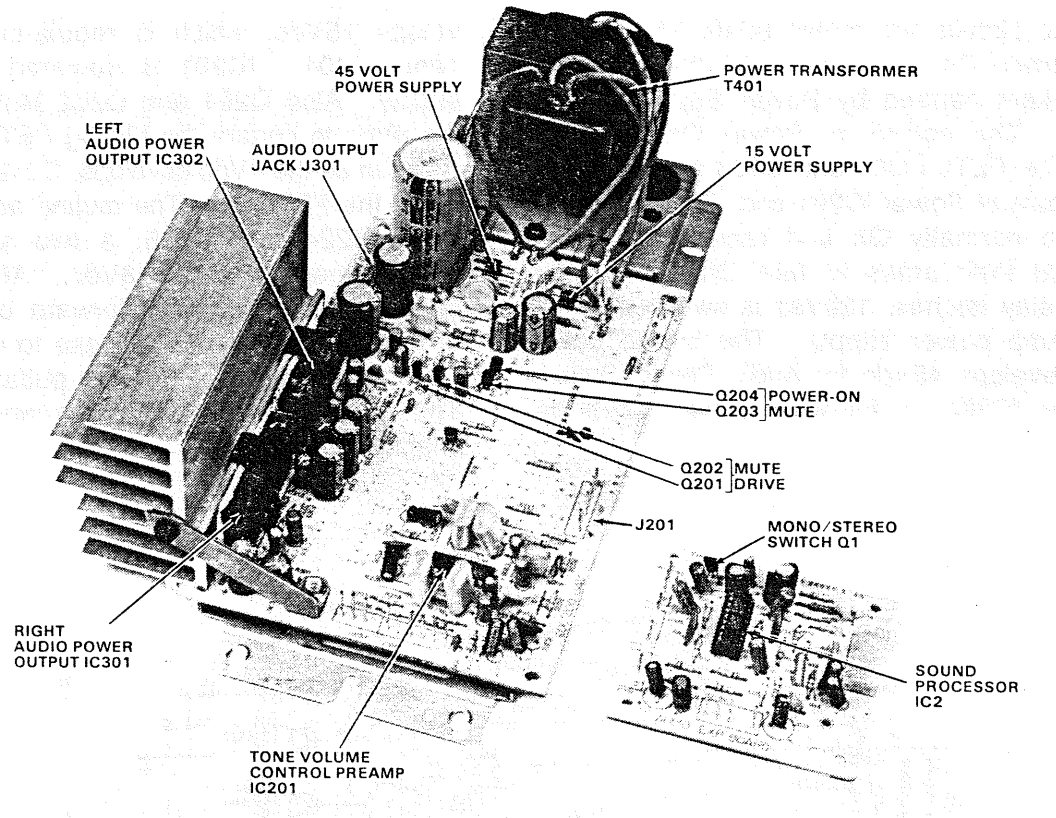


Figure 27- Sound Processing Module

Sound Processing Module & Stereo Amp

The Sound Processing Module and the Stereo Amplifier are shown in **Figure 27.** Callouts identify the major components and their functions. The 45Vdc and 15Vdc Power Supplies are located near the Power Transformer T401. Q203 and Q204 Turn-On Mute devices are near the center. Q201 and Q202 Mute Drive transistors are to the left of center and the Tone/ Volume Control IC201 is in the lower right. Audio Power Output IC301 and IC302 are located on the heatsink in the lower left. The Audio Output jack J301 is located above the Power IC's heatsink. The Sound Processing Module is plugged into the Power Amp jack J201. The major devices on this module are Q1 Mono/Stereo Switch and IC2 Audio Processor.

Figure 28 shows the Sound Processing Logic Encoder. When ac Power is turned On, IC2-14 outputs 12Vdc, which turns On the Mono switch Q8. D5 becomes forward biased and couples 12Vdc to the Sound Processing Module.

Left and Right Audio signals from the Input/ Output Panel J718-4-1 are fed to the Sound Processing Module through J1104-1, -4 to IC2-2, -17, **Figure 29**, Q1 stays On and connects IC2-2 to IC2-17, producing Monaural Audio at the Sound Processor IC2 inputs. Simultaneously, a logic High from the Tuner Interface Panel is fed to IC2-11, and a logic Low is fed to IC2-12 which maintains the Mode Select switches in the Monaural position. The Audio signals flows from IC2-2, -17 through the two Plus Amplifiers, the ModeSelect switches, and the Plus Output amplifiers of each channel to output Pins 6 and 13 respectively.

The Monaural Audio signal from the Sound Processing Module, **Figure 30**, is fed to the Pre-Amp IC201-15, -4. Bass, Treble and Balance control contour the frequency response and Audio balance. Audio signals fed from IC201-11, -8 drive IC302-5 and IC301-5 Power Output ICs. Output signals from IC302-9 and IC301-9 are fed to the speaker output jacks.

The Audio circuits are muted briefly when power is first turned On to prevent a "thump" heard in the speakers caused by Power Supply voltage build-up. The control of Power On Muting is provided by FETs Q204 and Q203 and is applied to the inputs of Power IC301 and IC302. The two FETs are normally On and require a positive voltage at their gates to turn Off. When the Power Relay latches, 120Vac is switched to the Stereo Amp power supply. The bridge power supply develops 45Vdc for Audio Power Outputs IC301 and IC302. A full wave power supply develops 15Vdc, which is regulated to 8Vdc by zener Z401. IC201 is powered by the 8Vdc supply. Also Q201 and Q202 Mute Drivers use the 8Vdc to control the Muting FETs Q203/Q204. As soon as the 8Vdc develops, Q202 saturates and holds the FETs On. The muting action continues while R224 and C225, a two second timing circuit, charges toward 8Vdc. After about two seconds, Q201 base is forward biased. Q201 turns On, and pulls Q202 base to ground. Q202 turns Off, and FET gates are pulled up by R222. The FETs turn Off, which un-mutes the Audio channels.

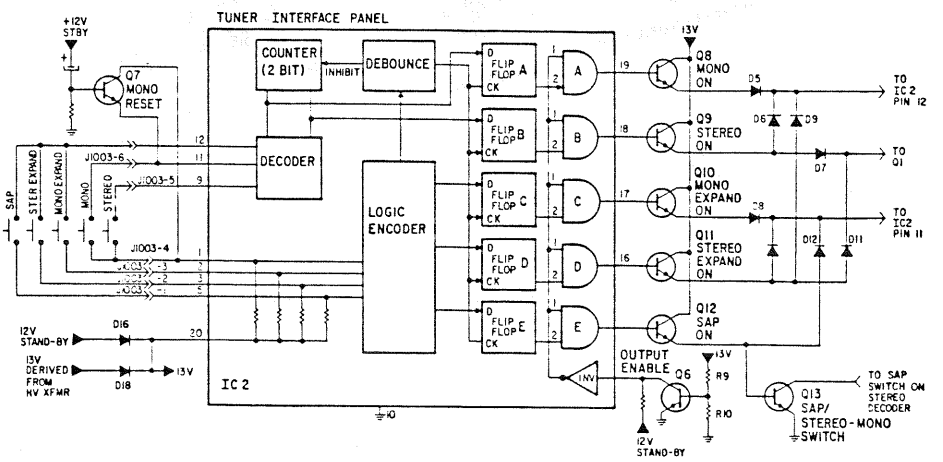


Figure 28- Sound Processor Logic Encoder

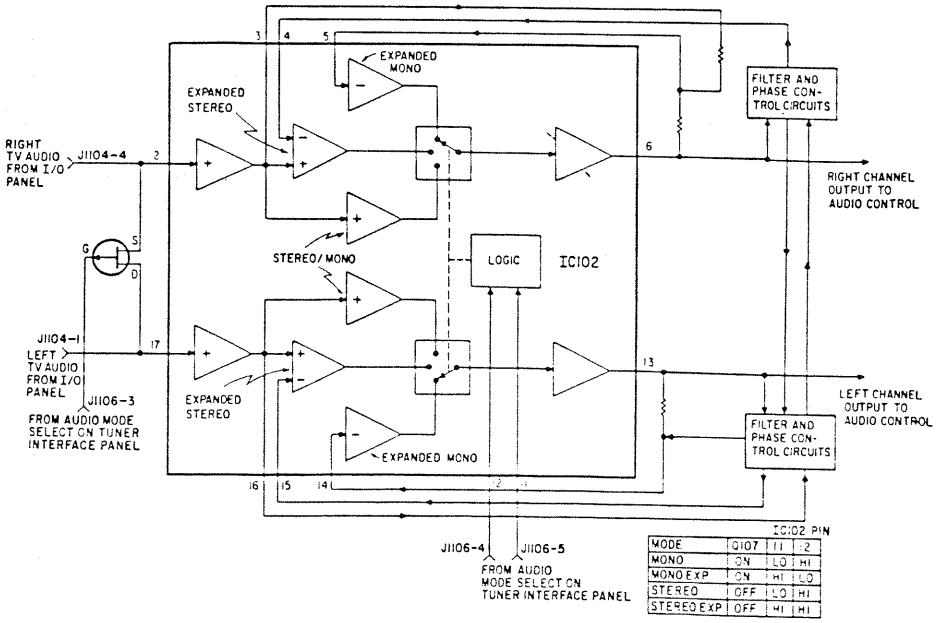


Figure 29- Sound Processing Circuit

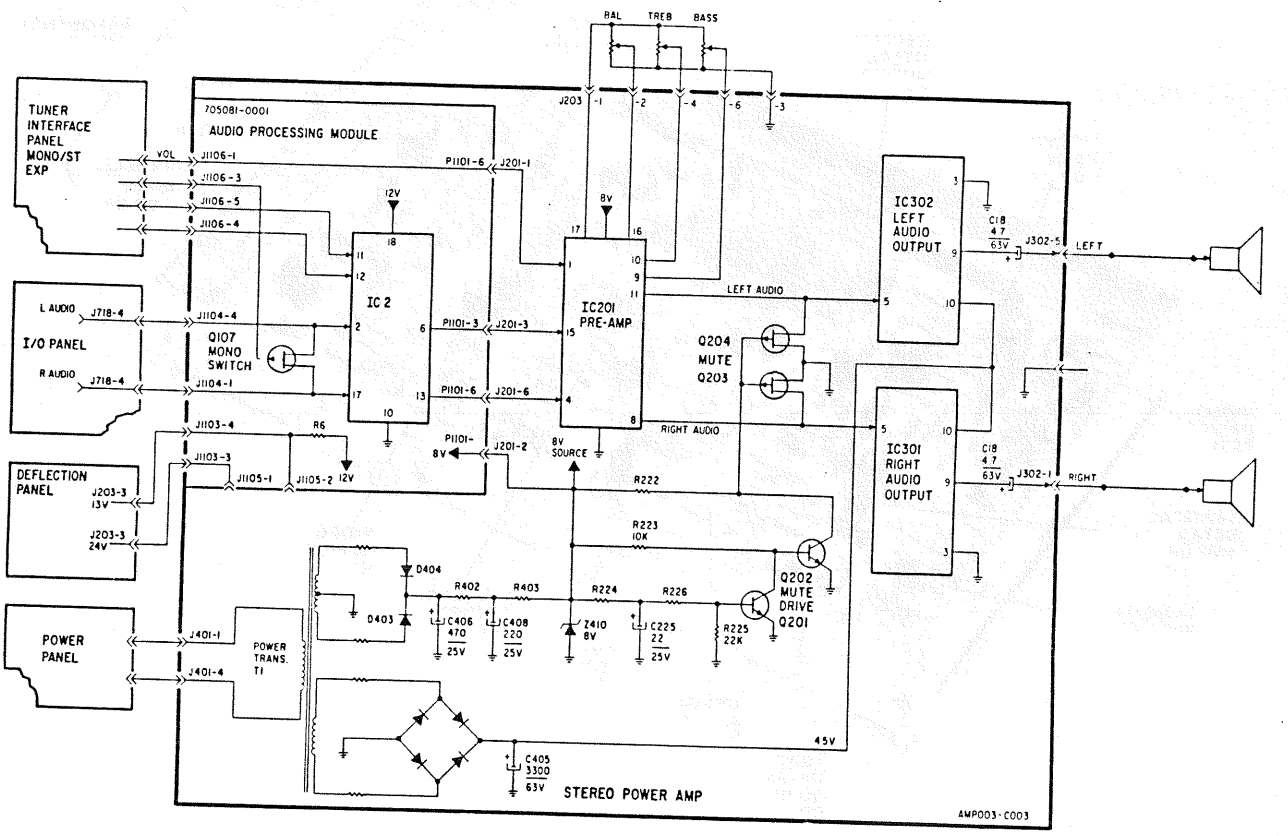


Figure 30- Stereo Power Amplifier

Comb Filter Module

The Comb Filter Module components and functions are illustrated in **Figure 31**. They are J501 Video Input Jack, Q2 Video Amplifier, Q8 Vertical Detail Buffer, IC1 Video/Chroma Comb Processor, RP1 Chroma Adjust, RP2 Luminance Adjust Q5, Q9, Q10, and Q11 Frequency Tripler transistors, Q3 Video Buffer, Q4 Mixer Amplifier, and RP3 Vertical Detail Adjust.

Refer to **Figure 32**. When the 1Vpp Video signal and the 1Vpp 10.74MHz Clock signal are fed to IC1, processing is synchronized by the Clock signal. Three signals are out: Pin 21 outputs Combed Video, Pin 13 outputs Vertical Detail Video and Pin 14 outputs Chroma.

Combed Video is fed to the 4.5MHz Filter FL2-1 input. FL2 removes residual Sound carrier energy and exits a 1Vpp Composite Video signal from FL2-3/TP4. Q3 buffers the combed and filtered Video and feeds it to Q4 base. The Vertical Detail Buffer Q8 drives Q6 with 0.5Vpp Vertical Detail signal to replace vertical resolution lost during the Video combing process. Q6 Vertical Detail gain is adjusted with RP3 and fed to Q4 Mixer base. The combed and filtered Video is matrixed with the Vertical Detail Video at Q4 base. Q4 collector outputs 1.2Vpp Vertical Detail Enhanced plus Video signal to the Video Processor Panel J416-5, and Q4 emitter outputs a 0.5Vpp Enhanced Video signal to J416-6.

Vertical Detail refers to the low frequency Video components that produce sharp vertical transitions between horizontal black and white lines. Restoration of vertical resolution, partly lost in the combing process, is accomplished by feeding full-bandwidth Composite Video through a 0-to-1MHz low pass filter and re-inserting this bandlimited signal with combed Luminance. The amount of low frequency Video re-inserted is controlled by the Vertical Detail Gain adjustment RP3. Improperly adjusted gain produces either a black or white horizontal line at the transition.

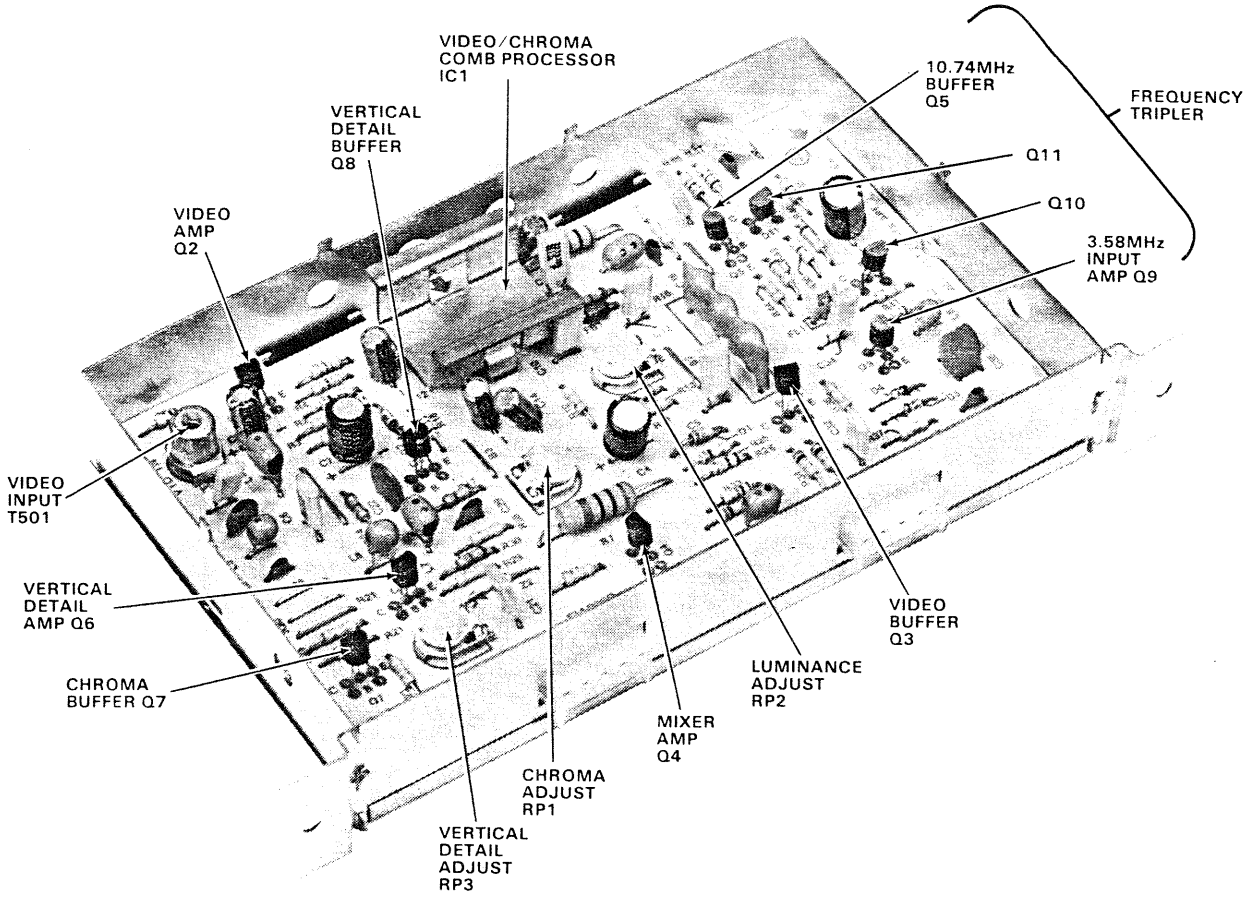


Figure 31 - Comb Filter Module

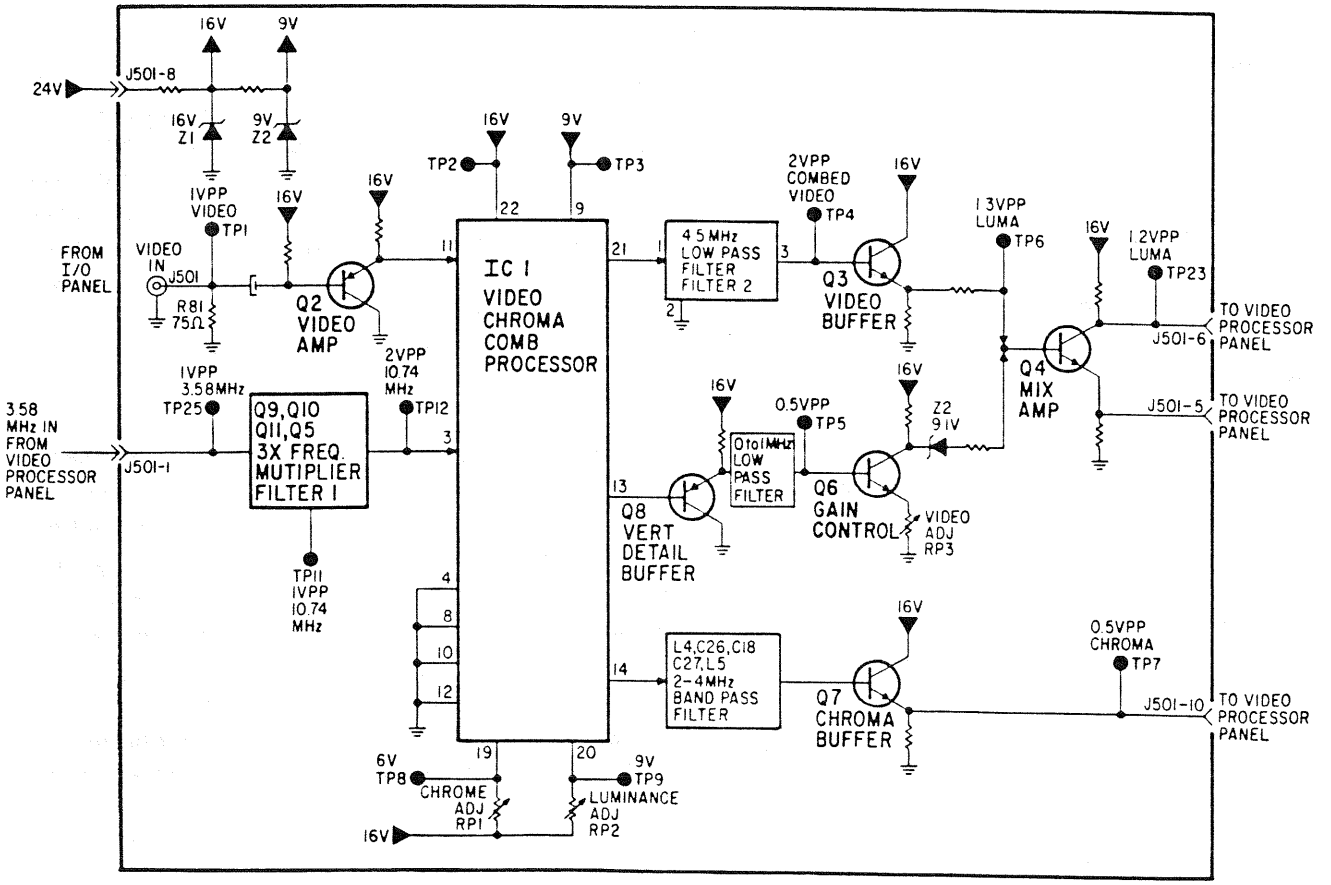


Figure 32- Comb Filter Circuit

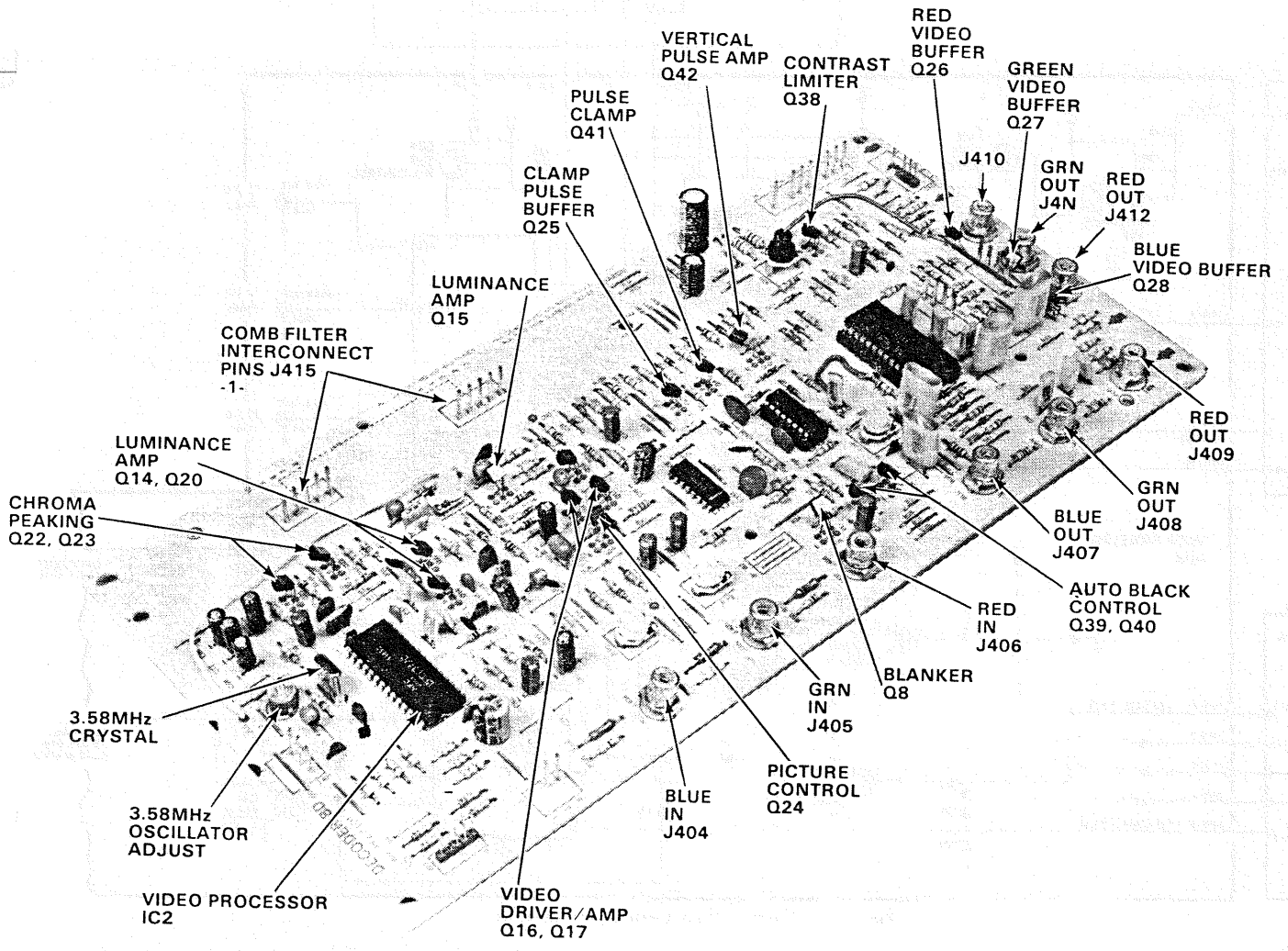


Figure 33 - Video Processor Panel

Video Processor Panel

Figure 33 shows the Video Processor Panel and the major components: Input/Output Jacks, transistors, ICs and controls. The jack functions are: Blue, Green and Red Outputs J404/J405/406, Blue, Green and Red Inputs J407/J408/J409 and Red, Green and Blue Outputs J410/J411/J412. The ICs and their functions are: IC2 Video Processor, IC6 RGB Buffer, IC5 Sand castle, and IC4 RGB Processor. The transistors and their functions are: Q14/Q20 - Video Amplifier, Q15/Q16/Q17 + Video High Frequency Amplifiers, Q13/Q18 Blankers, Q22/ Q23 Chroma Amplifiers, Q25 Clamp Pulse Buffer, Q26/Q27/Q28 Red, Green, Blue Video Output Buffers, Y1 3.58MHz Crystal, and C71 3.58MHz Oscillator tuning capacitor.

Auto Sharpness Control Circuit

Positive and negative Video and Chroma signals are fed from the Comb Filter to the Video Processing Panel, **Figure 34**. Positive Video high frequencies passed by C19 are buffered by Q15. Horizontal and Vertical Blacking pulses are added and the high frequency signal is coupled to Q16. The signal peaks are filtered by C46. The dc output from Q1 is applied to the control line from the Sharpness control to IC2-4. The customer Sharpness control sets the amount of high frequency peaking added to the Video signal and the Auto Sharpness circuit within IC2 maintains this setting.

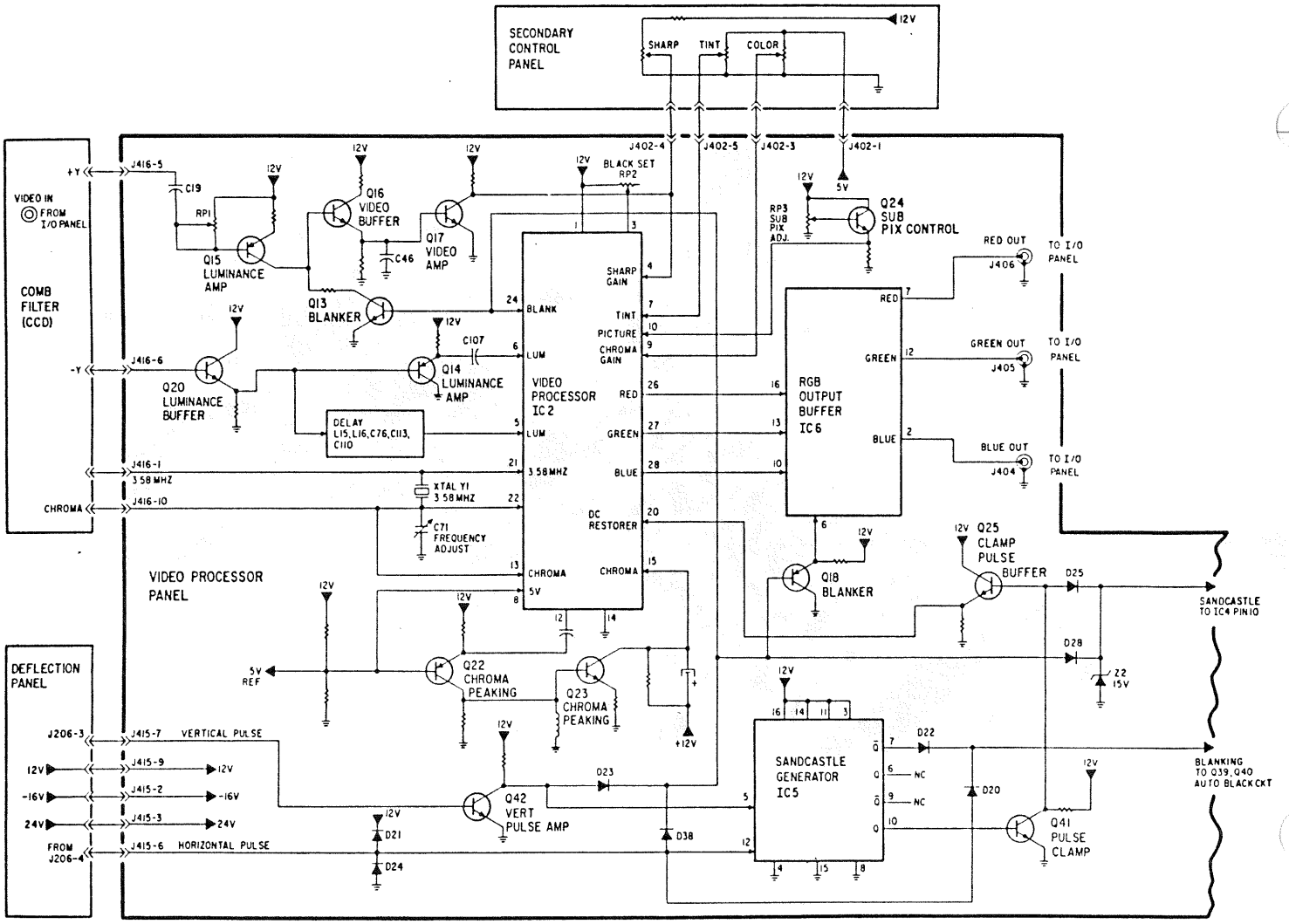


Figure 34 - Video/Chroma Processing Circuits

Video Processing Circuits

Negative Video from the Comb Filter J416-6 is fed to Luminance Buffer Q20, which feeds Video to the Delay Circuit L15/L16, C76/C110/C113, and Q14 Luminance Buffer. The delayed Video is coupled to IC2-5. The Q14 buffered Luminance signal, limited to high frequencies by C107, is coupled to IC2-6. These two signals are combined within IC2 and produce an image enhancing Video signal. This signal is gain adjusted by the dc voltage at IC2-10 from the Sub-Picture control RP3/Q4 and the associated circuitry. Proper picture contrast setting occurs when IC2-10 is about 8Vdc.

Chroma Processing

The Chroma signal from the Comb Filter J416-10 is fed to IC2-13. Chroma gain is adjusted by the dc voltage fed to IC2-9 from the Color control on the Control Panel. Maximum color occurs when IC2-9 is 5Vdc. The tint adjustment is made by changing the dc voltage at IC2-7 with the Tint control. The normal setting for good flesh tones is about 2Vdc.

Internal matrixing of the demodulated Chroma and the dc restored Video with Blanking added develops the 4Vpp R, G, and B Video signals fed to the RGB Buffer IC6. Composite Blanking is fed to IC6-6 to remove the Blanking inserted at the Video Processor IC2-24. The R, G and B Video signals, less Vertical and Horizontal Blanking, are to the I/O Panel and back for additional processing by the RGB Processor IC4.

Sand Castle Generator

The Sand Castle Generator produces a specialized waveform consisting of Vertical and Horizontal Blanking pulses with a narrow Clamp Pulse located on the back porch of the Horizontal pulse, where Burst would normally be located. The Horizontal and Vertical pulses are used to re-

insert Blanking in the Video signals and the Clamp Pulse is used for dc restoration.

The Sand Castle circuit is composed of a dual Flip Flop IC5, Pulse Clamp D21/D24, Pulse Clamp Q41, Clamp Pulse Buffer Q25, Vertical Pulse Amplifier Q42, and Matrix diodes D28/D25 and D20/D22. Flip Flop IC5-12, triggered by fly-back pulses clamped to 12Vdc, outputs four microsecond 12Vpp pulses at IC5-10. The pulses are fed to Q25, buffered, and sent to IC2-20. The pulses clamp the Video signal and re-insert the dc component that was lost in ac coupling to IC2-5, -6.

The four microsecond pulses are mixed with the 2Vpp Horizontal pulses to develop the 6Vpp Sand Castle signal. Horizontal and Vertical Blanking pulses are combined through diodes D20 and D22 to produce the Composite Blanking signal.

RGB Processing Circuits

The RGB Processing circuits, seen in **Figure 35** include IC4 and its R, G, and B inputs J409/ J408/J407, Auto Black Level transistors Q39/ Q40, Peak Contrast control Q38, Picture and Brightness controls RP1/RP2, and Fail Safe circuit diodes D30/D31/D32.

The R, G, and B signals are ac coupled from the Input/Output Panel to IC4. As a result, dc restoration, black level adjustments, and blanking reinsertion must be performed. The Sand Castle signal is applied to IC4-10. The narrow pulse occurring during the Horizontal Blanking interval is used to clamp the back porch of RGB Horizontal Blanking to restore the dc reference level. The Composite Blanking pulses are coupled through the Auto Black transistors Q39 and Q40 to IC4-20 to restore Vertical and Horizontal Blanking to the Video signal for CRT blanking.

Black level is a preset dc voltage adjusted by Sub-Brightness control RP4, which is a preset dc voltage adjusted by Sub-Brightness control RP4, which sets the IC4-20 voltage and IC4 R, G, and B gain. The Peak Contrast Limiter Q38 monitors the R, G, and B outputs IC4-1, 3, 5 through diodes D13, D14, and D-15. Positive peaks of the R, G, and B Video signals exceeding the threshold set by RP5 turn On Q38 and reduce the gain during peaks. RP5 is adjusted for 2V pp Video drive at CRT Panel J803, which develops 100Vpp drive at CRT cathode pin 4.

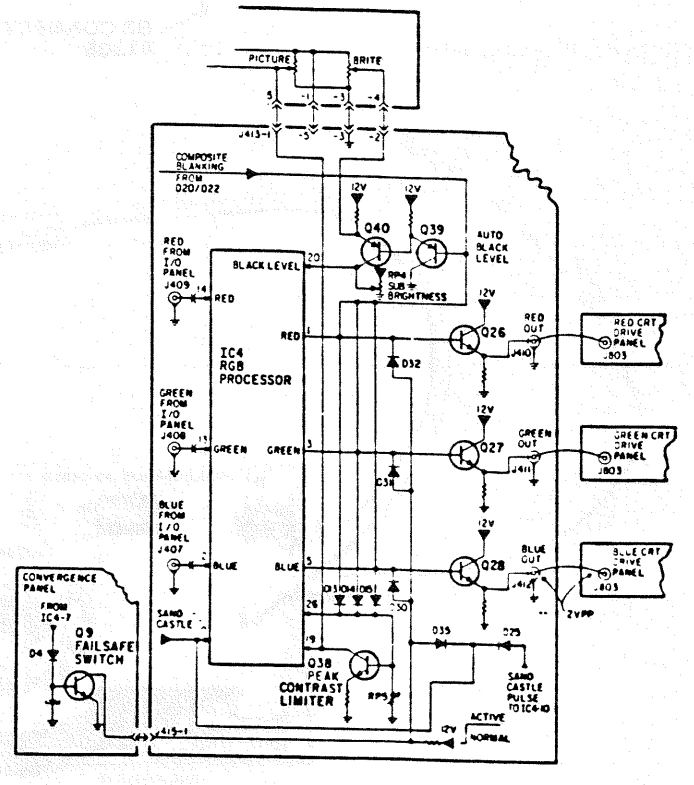


Figure 35 - RGB Processing Circuits

The Auto Black circuit drive signal is composed of Vertical pulses from IC5-7 and Horizontal pulses from the input to IC5-12. This Composite Blanking signal is clamped to 12Vdc by IC5, and the Horizontal pulses are clamped by diodes D21 and D24 at IC5-12.

Vertical Sweep Fail Safe Circuit

The Fail Safe Switch Q9 and 12Vdc are connected to the RGB Outputs through D30, D31, D32 and to D35, which is connected to the Sand Castle circuit. During normal operation, the Vertical Ramp is present at the Vertical Waveform Amplifier IC4-7 on the Convergence Board. Diode D4 rectifies the ramp, which turns On Q9. Q9 grounds the anodes of D30, D31, and D-32, and D-35 becomes reverse biased. However, when Vertical Drive to D4 disappears, Q9 is turned Off and the anodes of D30, D31 and D32 are lifted from ground. D35 is turned On, which elevates the Sand Castle line above the Blanking level. The RGB Processor IC4-10 sees the new DC voltage and blanks the Video IC4-1, -3, -5 outputs no Video and the DC level cuts Off the CRT beam currents.

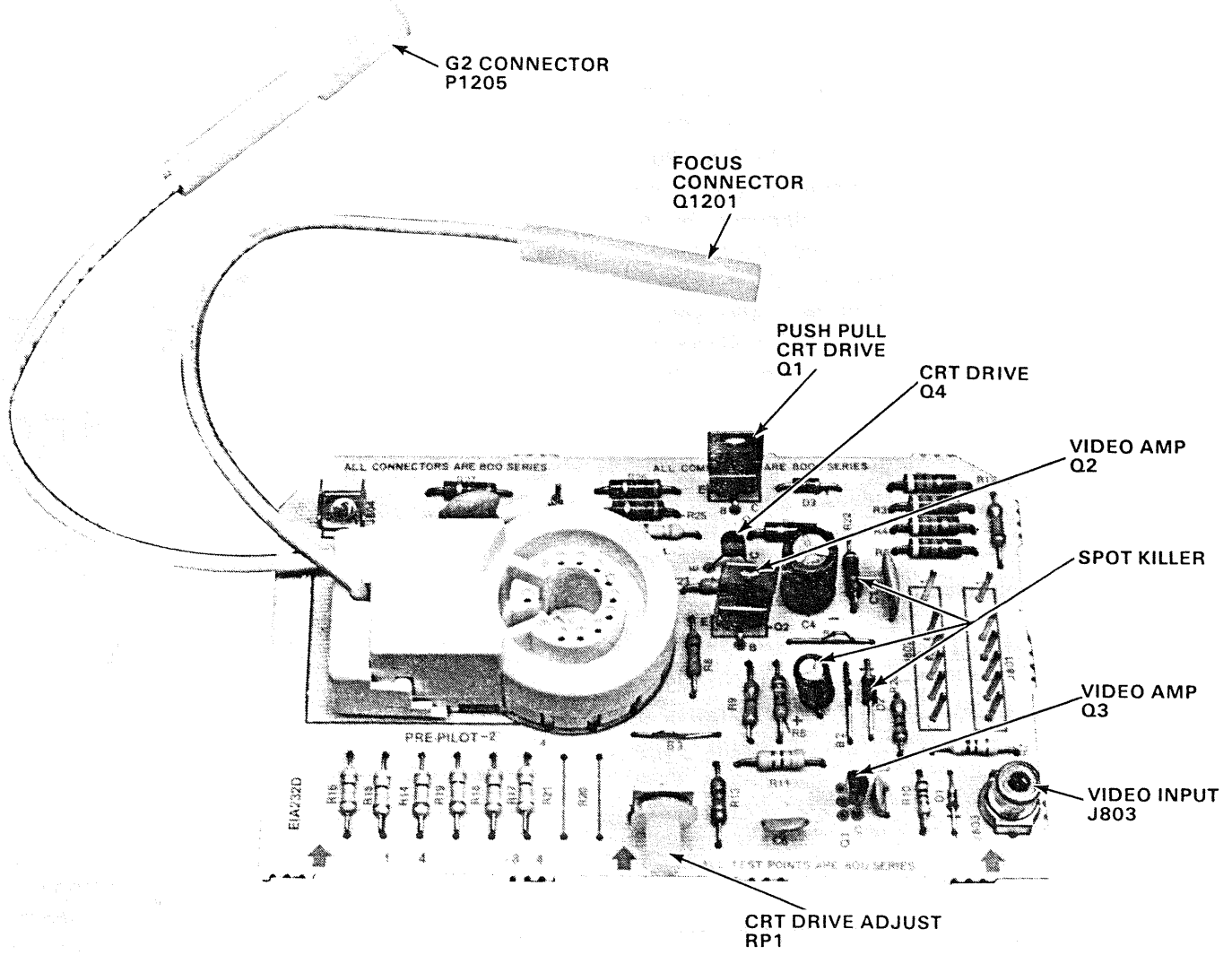


Figure 36 - CRT Drive Panel

CRT Drive Panel

There are three Drive Panels, all of which are identical in circuitry and component layout, **Figure 36.** The major components are: G2 and Focus leads, Push Pull CRT Driver Q1/Q4, Video Amplifiers Q2/Q3, and CRT Drive Adjust RP1.

After color signal decoding, the Sync and 2Vpp R, G, and B Video signals are fed to their respective CRT PAnels. In **Figure 37**, the Blue Video signal is shown coupled to J803 and amplified by Q3/Q2 (Q2 serves as part of the Q3 collector load). Q3/Q2 outputs 100Vpp inverted Video to the Q1/Q4 push pull amplifiers, which drive the cathode of the Blue CRT with 100Vpp Sync-positive Video.

When the set is turned Off, or when ac power is interrupted, or when Horizontal and Vertical sweep voltages are removed because of a shut-down condition, the CRT beam currents could produce a high-intensity spot on the faceplate and permanently damage the phosphor coating. This possibility exists because 30KV anode voltage is still present for a short period after the power supplies have been turned Off. The Spot Killer circuit protects the CRTs by cutting Off beam current whenever one of these interruptions occurs.

When the set is turned On, 200Vdc is developed by the power supply and fed to the CRT Panel circuits through J801-1. In the Spot Killer circuit, the negative end of the capacitor C4 is grounded through conducting diode D2. C4 charges to the full 200Vdc supply. D2 remains forward biased as long as the supply voltage is

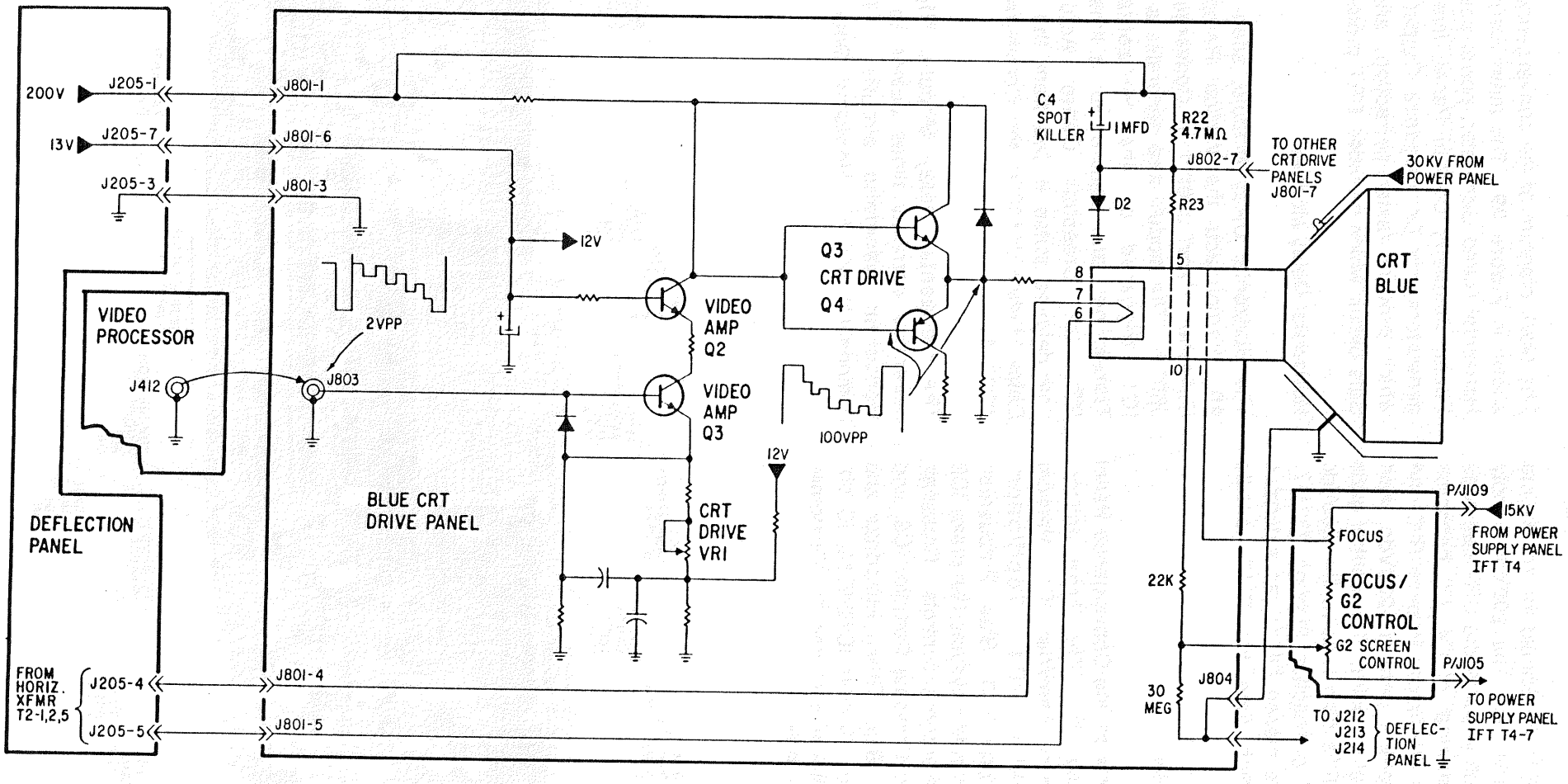


Figure 37 - CRT Drive Circuit

present at the top of R22. Should the set go into shutdown or be turned Off, the 200Vdc supply decays to zero, which grounds the CRT cathodes and the positive terminal of C4; D2 becomes reverse biased. C4 discharges through R22 and places the CRT control grid at -200Vdc, well beyond the beam cut-off point. The control grids of the other two CRTs also receive the 200Vdc due to the parallel connection through J801-7. The three CRTs are biased Off for an extended period, during which time the 30KV anode voltage discharges.

Convergence Circuits

The main components on the Convergence Panel are shown in **Figure 38.** The Panel utilizes Horizontal Waveform Amplifier IC1, Vertical Waveform Amplifier IC4, Top/Bottom Pincushion Generator IC3, Side Pincushion Generator IC5, Trapezoid Keystone Generator IC2 and associated convergence controls. Crosshair Generator IC9, Zero Crossing Detector IC8, and Fail Safe Q9, Red, Blue, Green Horizontal and Vertical Convergence Outputs IC12/IC14, IC 10/ IC13, IC15/IC11 respectively, and the Customer Convergence Control Panel.

The block diagram of the convergence circuits is shown in **Figure 39.** The main circuits are: the Horizontal Ramp Generator, power source for the Panel, Customer Control Panel, five waveform generators, six Convergence Output Amplifiers which provide raster correction, and the Fail Safe circuit which provides CRT protection.

Horizontal Delay Module

The Horizontal Delay Module, seen in **Figure 40**, interconnects the Vertical Ramp from the Deflection Panel J202-1 to Convergence Panel J607-5. The module also generates a pulse from IC1, triggered by the Horizontal Output Transformer, and adjusted for a time delay by RP1, the Crosshair Center Adjust. The time-delayed pulse is fed from the Horizontal Delay Module J1102 to the Convergence Panel J607-5.

The Horizontal Delay Module, **Figure 41**, generates correctly times pulses to drive the Horizontal waveform circuits. The main components are: IC1 Horizontal Delay Flip Flop

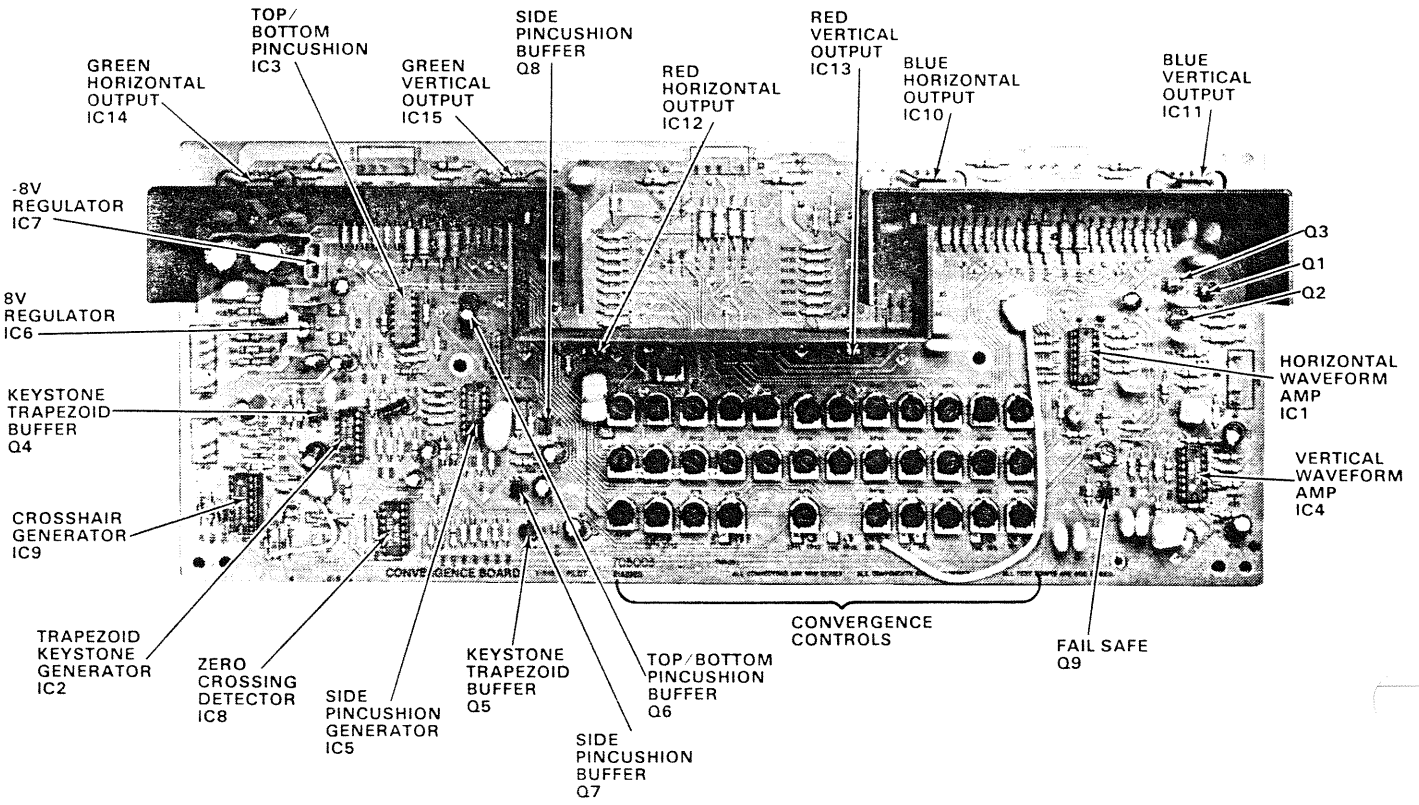


Figure 38 - Convergence Panel

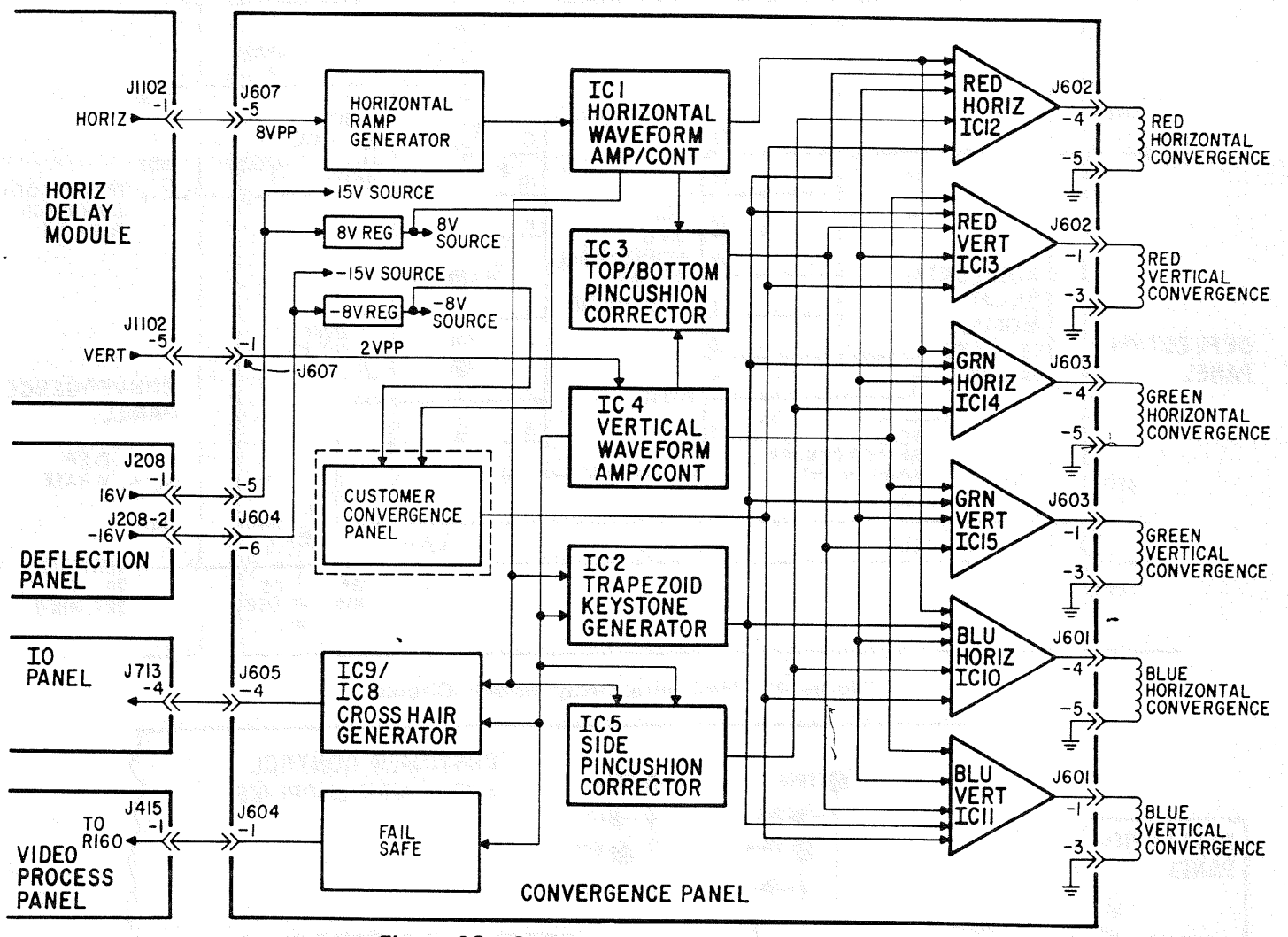


Figure 39 - Convergence Panel Block Diagram

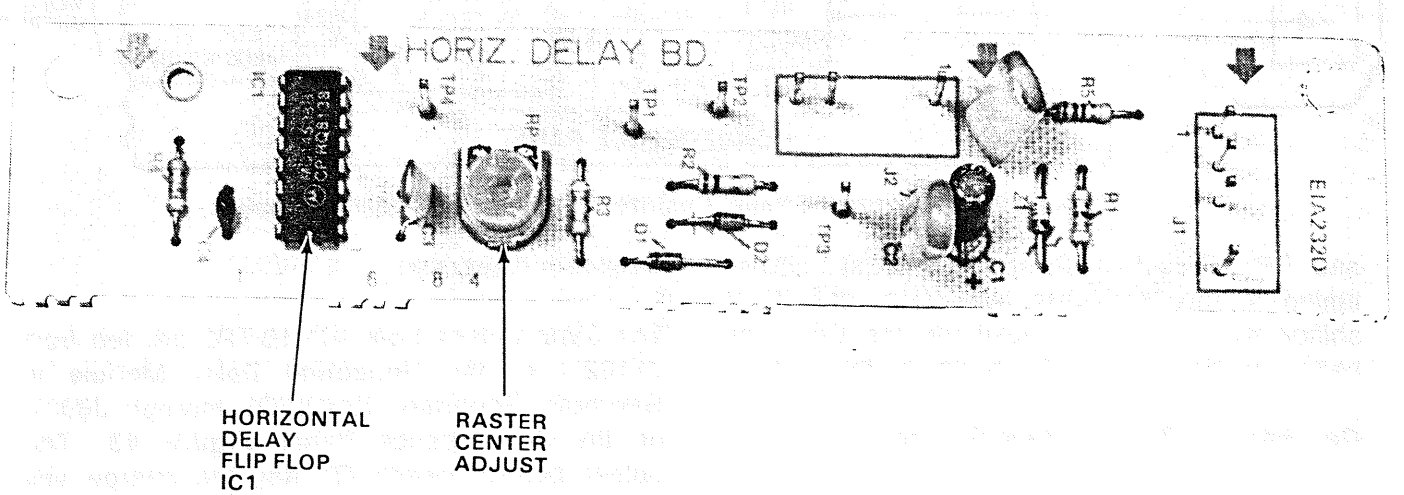


Figure 40 - Horizontal Delay Module

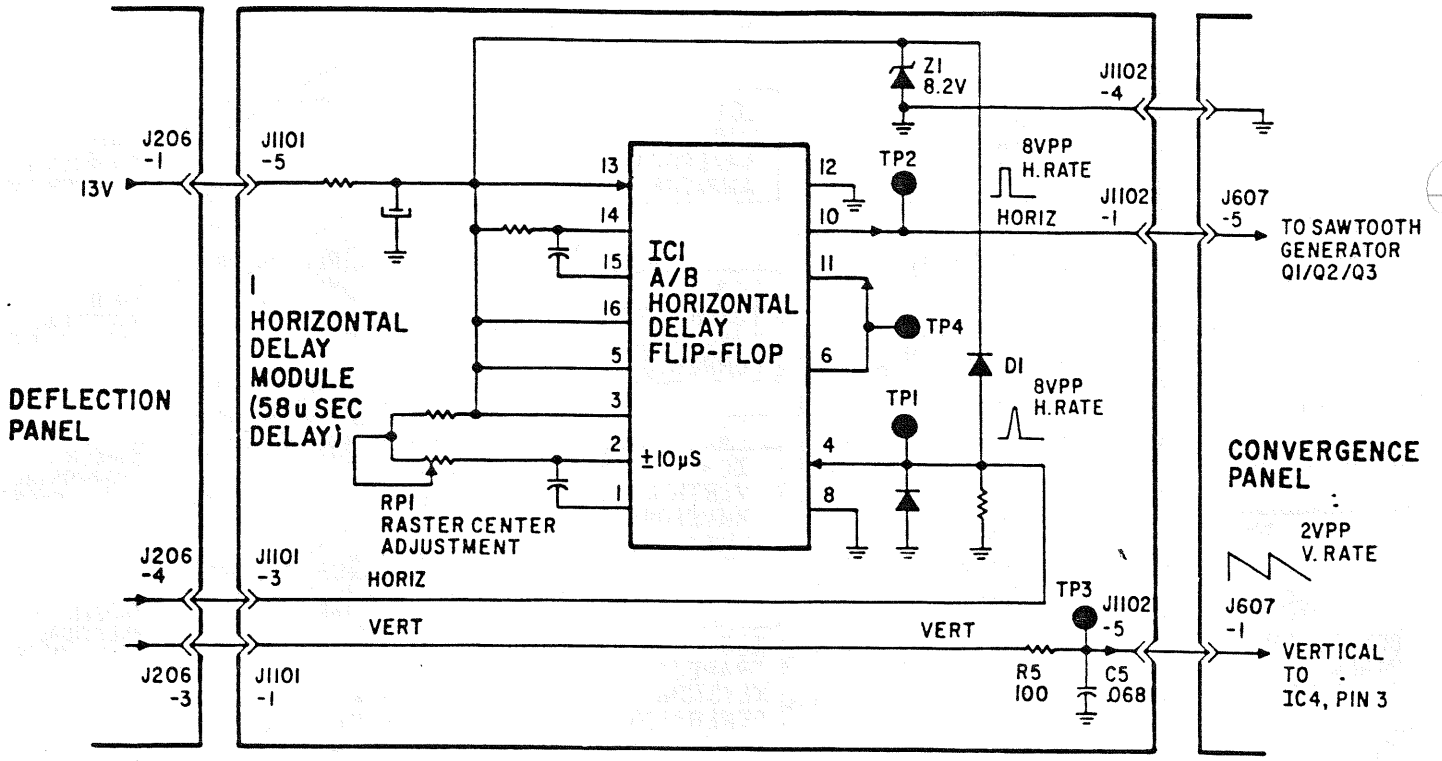


Figure 41 - Horizontal Delay Module Circuit

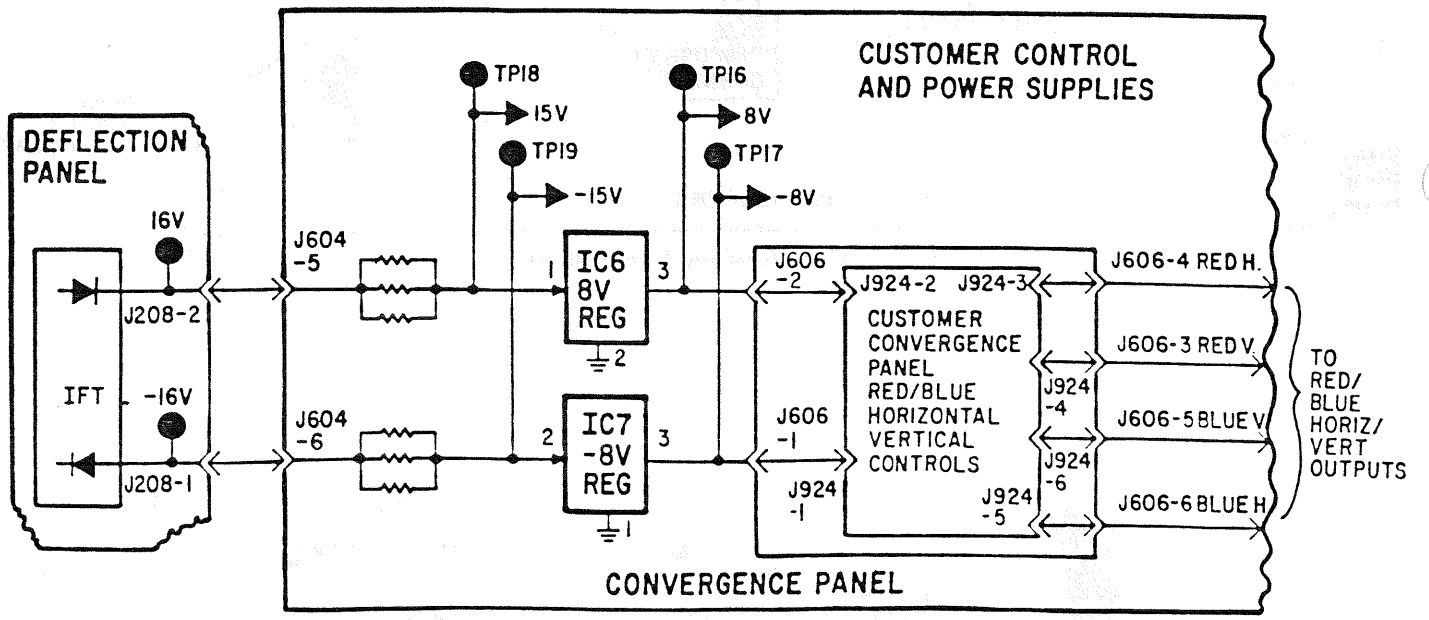


Figure 42 - Convergence Panel Customer Controls and Power Supplies

and RP1 Crosshair Centering Adjust. Pulse timing in the Horizontal waveform circuits is shifted by RP1, which positions the Crosshair pattern vertical line in the center of the raster.

Convergence Panel Voltage Source

The +16Vdc and -16Vdc from the Deflection Panel J208-1 and -2, **Figure 42**, are used to derive +15Vdc and -15Vdc for the Convergence Panel. IC6 and IC7, the Regulator ICs, use the scan derived dc voltages to develop +8Vdc and -8Vdc for the Customer Panel controls.

Sawtooth Generator

The 8Vpp pulses from IC1-10/TP2 are fed from J1102-4 of the Horizontal Delay Module to Sawtooth Generator Q1/Q2/Q3 through J602-5 on the Convergence Panel, **Figure 43**. The pulses control switch Q1 and the charge and discharge of sawtooth capacitor C1. The sawtooth is buffered by Q3 and processed into negative 0.2Vpp pulses by capacitor C4 to drive the Horizontal Waveform Amplifier.

Horizontal Waveform Amplifier

The negative pulses from capacitor C4 drive IC1-2, **Figure 44**. The negative pulses are processed into a 3Vpp negative sawtooth at IC1-1/TP2 and a positive 3Vpp sawtooth at IC1-7/TP3. Both waveforms are fed to controls RP1, RP2, RP3, RP4, RP5, and RP6. The sawtooth waveforms from TP2 and TP3 are processed by IC1 into parabolic waveforms. A positive 1.5Vpp parabola is output from IC1-8/TP4 and a negative 1.5Vpp parabola is output from IC1-14/TP5. Both waveforms are fed to control RP12, RP13, RP14, RP15, RP16, and RP17.

Vertical Waveform Amplifier

The Vertical Waveform Amplifier IC4, **Figure 45**, is derived by a 2Vpp negative Vertical sawtooth fed from the Horizontal Delay Module J1102-5. IC4 processes the Vertical sawtooth into a 4Vpp positive sawtooth at IC4-1/TP11 and a negative 4Vpp sawtooth at IC4-7/TP12. Both waveforms are fed to controls RP20, RP21, RP22, RP23 and RP24. Parabolic waveforms are developed by IC4 sawtooth processing. A positive 4Vpp parabola is present at IC4-8/TP9 and a negative parabola appears at IC4-14/TP10. Both signals are fed to controls RP25, RP26, RP28, and RP33.

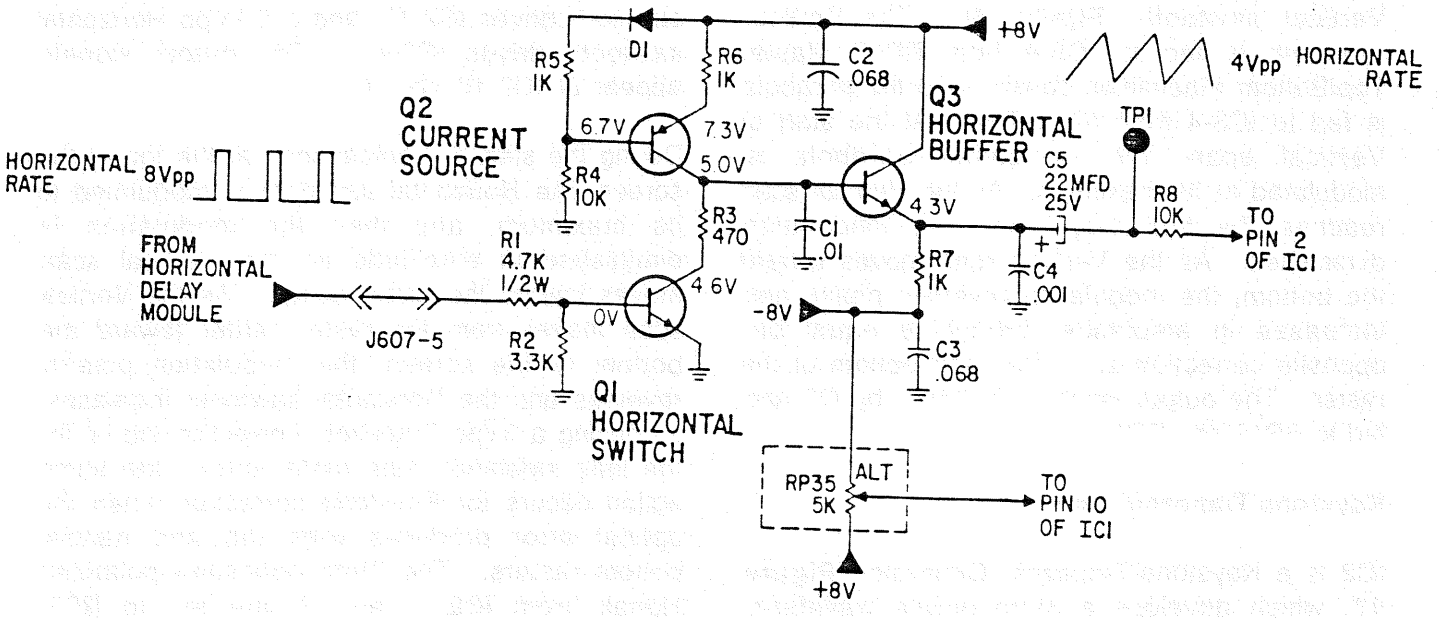


Figure 43 - Sawtooth Generator

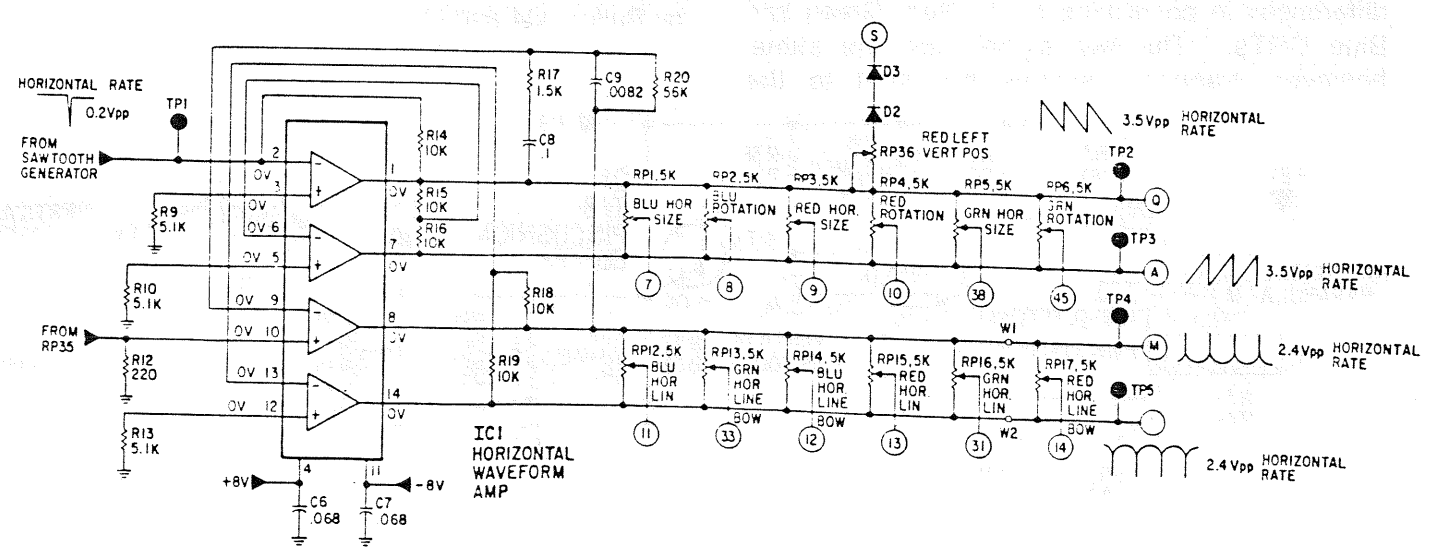


Figure 44 - Horizontal Waveform Amplifier

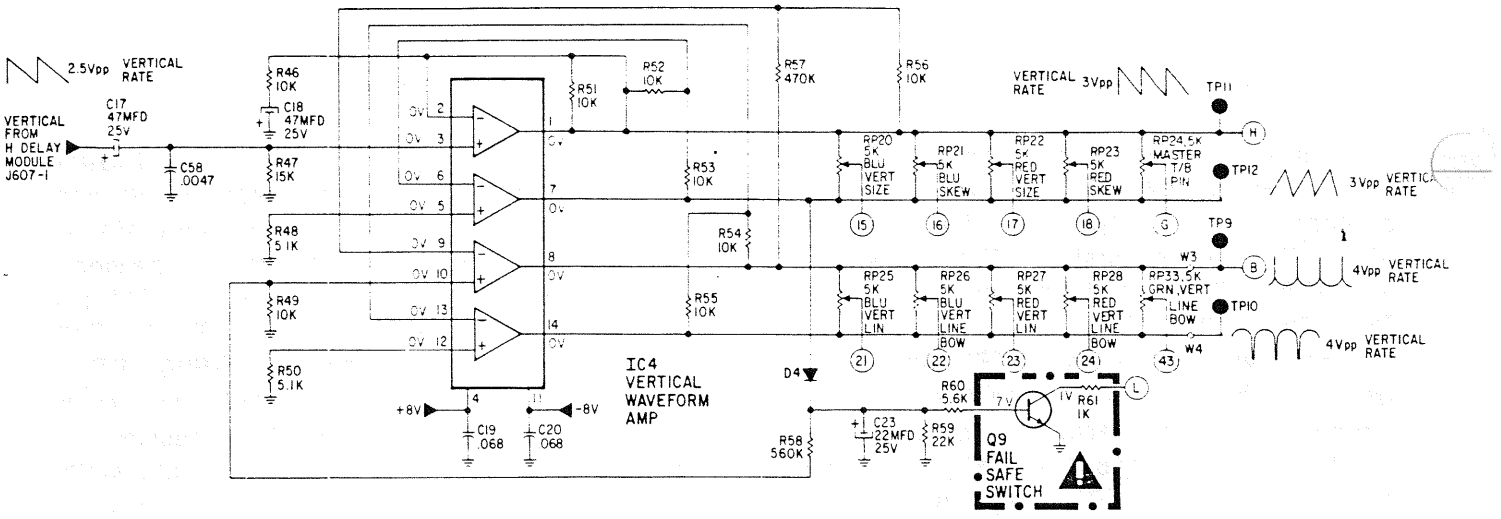


Figure 45 - Vertical Waveform Amplifier

Top/Bottom Pincushion Generator

IC3 is a Modulator/Inverter which modulates a 2Vpp Horizontal parabola with a 0 to 6Vpp Vertical sawtooth, **Figure 46**. The Vertical sawtooth is fed to IC3-9 from RP17 Master Top/Bottom Pincushion control, and the parabola is fed to IC3-4 from IC1-8/TP4. At the start of Vertical scan, the Horizontal parabola is modulated to its maximum. As the Vertical scan reaches the half way point, the modulation diminishes. As the Vertical scan moves toward the bottom, the modulation reverses phase and increases in amplitude, producing equal but opposite correction at the top and bottom of the raster. The output signal is buffered by Q6 and fed to RP19 and RP18.

Keystone/Trapezoid Generator

IC2 is a Keystone/Trapezoid Generator, **Figure 47**, which develops a 3Vpp bowtie waveform, used to correct raster error caused by the differences in positioning of the Red, Green and Blue CRTs. The two signals are the same; however, trapezoid signals are sent to the Vertical Convergence Amplifier, and Keystone signals are sent to the Horizontal Convergence Amplifiers. IC2 is driven by both Horizontal and Vertical sawtooth signals. A 1.5Vpp Vertical rate sawtooth drives IC2-10, and a 0.1Vpp Horizontal sawtooth drives IC2-4. The output signals appear at IC2-12 and -6.

During the start of Vertical scan at the top of the screen, the Horizontal sawtooth is modulated to its maximum, and then the modulation is diminished in amplitude ad the Vertical scan moves toward the raster center. As the Vertical scan moves from the raster center toward the bottom of the screen, the modulation polarity reverses and the Horizontal sawtooth increases, producing a 3Vpp Trapezoid correction signal for the long side/short side raster error. the same action occurs for Keystone correction when the optical error produces wide top and narrow bottom rasters. The 3Vpp oppositely-polarized signals from IC2-12 and -6 are fed to RP7, RP8, RP9, RP10, RP11 and test points TP6/7 by Buffers Q4 and Q5.

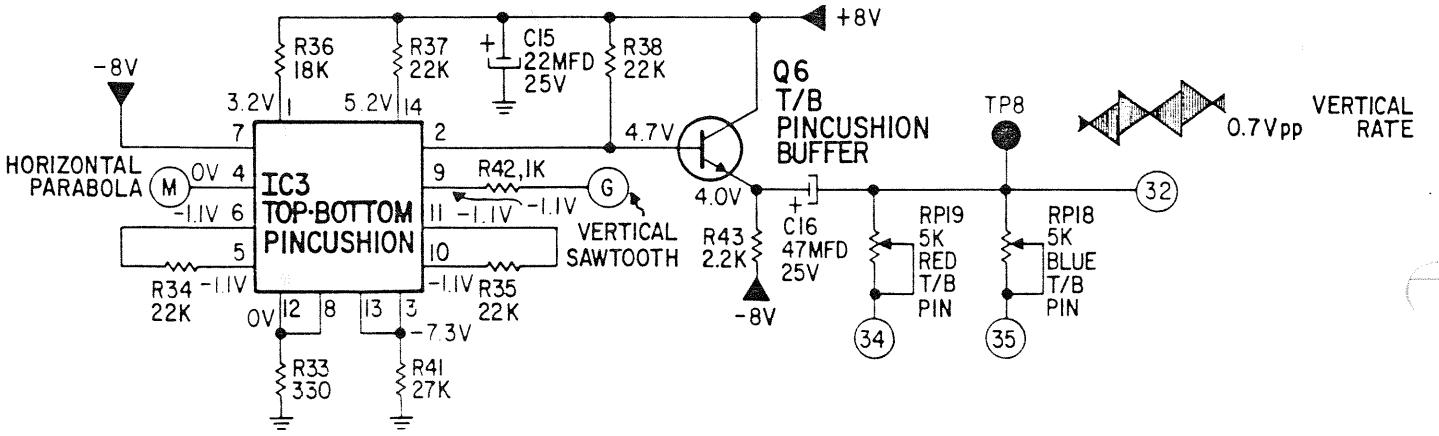


Figure 46 - Top/Bottom Pincushion Generator

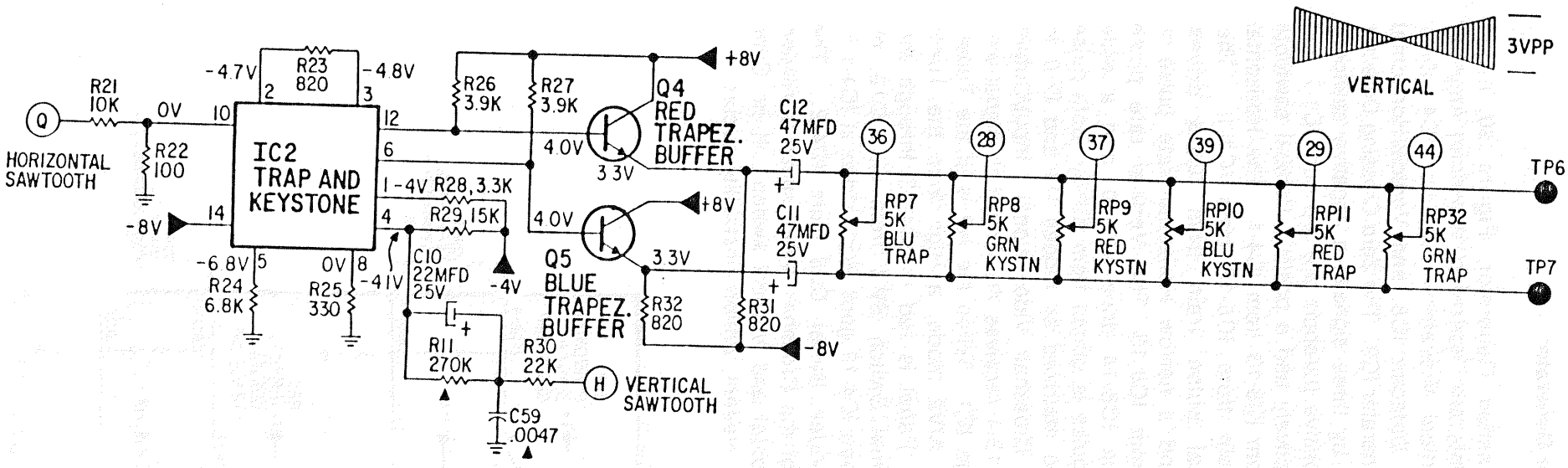


Figure 47 - Keystone/Trapezoid Generator

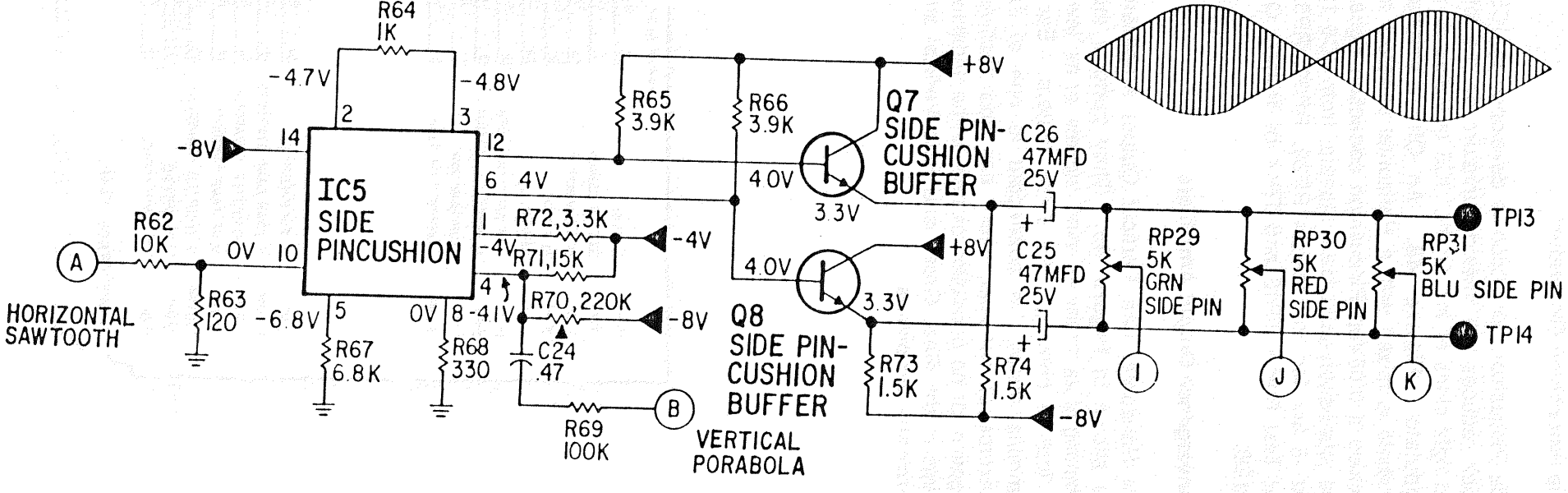


Figure 48 - Side Pincushion Generator

Side Pincushion Generator

Side Pincushion correction is developed by IC5, which reduces the inward curvature on the left and right sides of the raster. IC5 operates as a modulator, **Figure 48**. An Offset Vertical parabola is mixed with a Horizontal sawtooth to develop a 0.06Vpp Pincushion correction signal. The oppositely-polarized signals from IC6-12 and -6 are fed to controls RP29, RP30, RP32 and Test Points TP13 and TP14 by Buffers Q7 and Q8.

Convergence Output Amplifiers

The Horizontal and Vertical Output Amplifiers are shown in **Figure 49**. They perform the summing of as many as nine signals or as few as four to converge the three rasters. Each summing resistor is connected to one of 35 convergence controls, which can add positive, negative, or no correction signals to the summing points of the Red, Green and Blue Vertical and Horizontal Amplifiers.

Crosshair Generator

The Crosshair Generator, **Figure 50**, major components are: Horizontal Waveform Amplifier IC1, Vertical Waveform Amplifier IC4, Zero Crossing Detector IC8, and Vertical/Horizontal Pulse Generator IC9. The Zero Crossing Detector is driven by three signals: a negative sawtooth and a positive parabola are fed from IC1-7 and -8 respectively and a positive Vertical sawtooth is fed from IC8-13 from IC4-1. The Horizontal pulse train from IC8-13 from IC4-1. The Horizontal pulse train from IC8-8 drives IC9-2, and a narrow Horizontal rate pulse is output from IC8-13. The Vertical rate pulse train from IC8-14 drive IC9-10, and a wide Vertical pulse is output from IC9-5. Both pulse trains are matrixed by diodes D9 and D10 to form the Crosshair Video signal. Input/Output Panel J713-4 receives the Crosshair signal and feeds it to IC1. When the set is in the Tuner, A/V1, or A/V2 mode, a High from the Tuner Interface Panel is fed to IC4-13 through the Test/Normal Switch SW1 from D9,, D10, or D11. When IC4-13 goes High, Video at IC4-1 is fed to Video Buffer Q28 from IC4-2. The stability of the Crosshair Video signal is related to Horizontal and Vertical sweep. If no Sync signal is present, pattern instability occurs

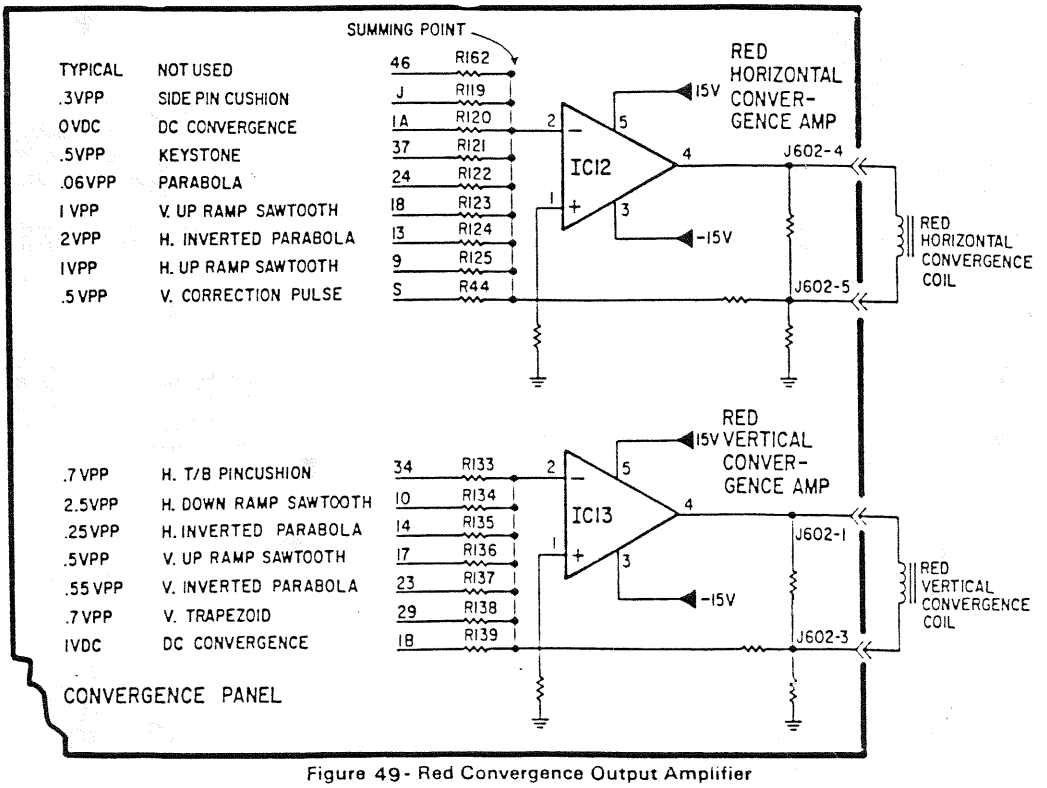


Figure 49- Red Convergence Output Amplifier

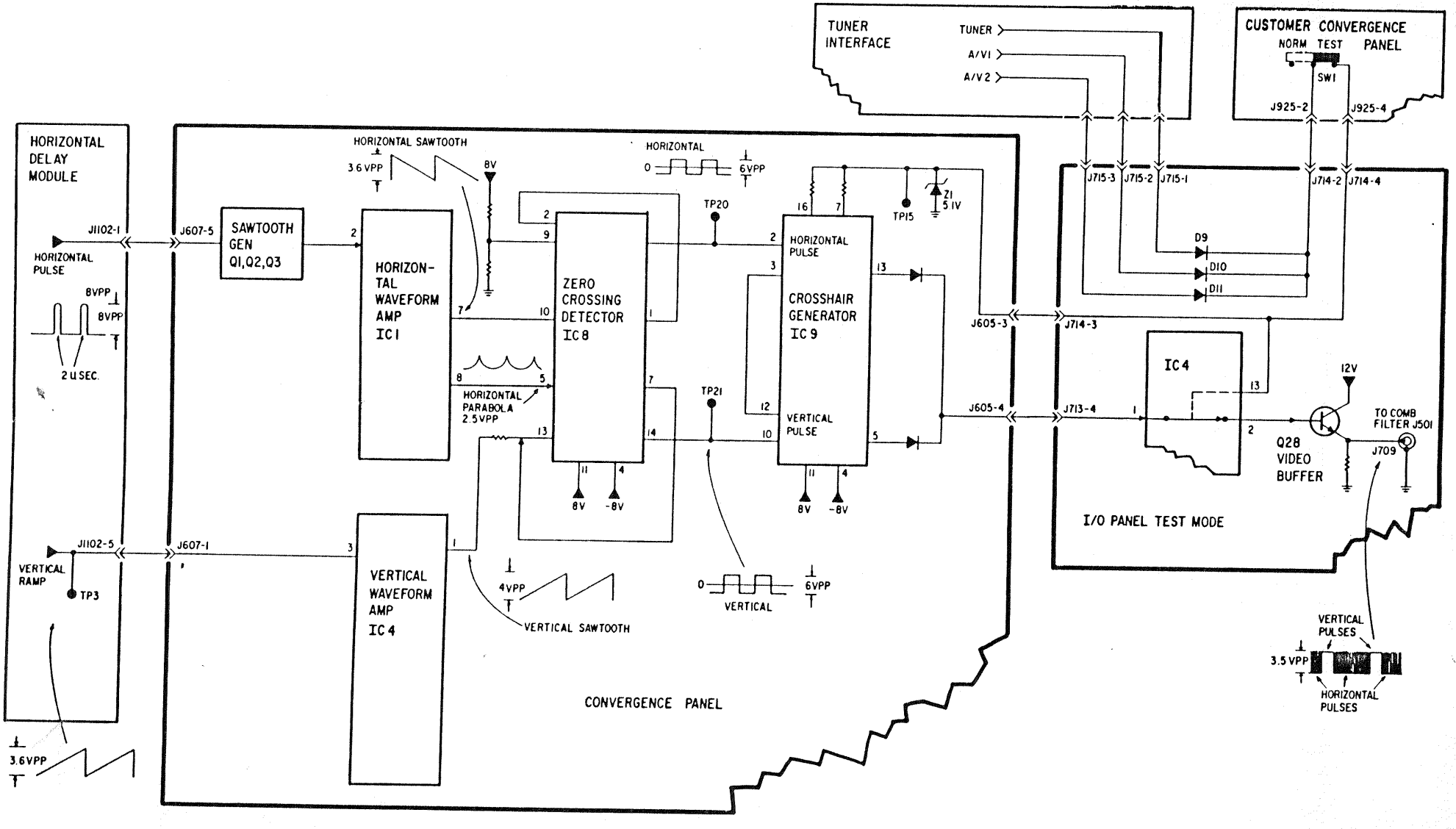


Figure 50 - Crosshair Generator